A Unique Timing-Reference System for Broadcast Videotape Recorders

By BERT H. DANN

A system for deriving timing pulses for the servo and time-base correction circuits of a videotape recorder is described in which digital techniques are extensively employed for maximum stability. These techniques provide a coordinated array of timing pulses which can be manually adjusted to accommodate cable and system delays and, in conjunction with other special machine features, can be moved automatically to provide error-free electronic editing.

General System Requirements; The Digital Approach

In order to produce an output which is fully synchronous with all other signals at the point where they are mixed and/or switched in a television system, a videotape recorder requires an array of internal timing references which are advanced in time with respect to the input synchronizing reference, to accommodate the inherent delays of the VTR. These delays include those of the lowpass filtering systems used in the video circuitry, certain minor delays which occur in the RF system, and the delays inherent in the time-base correction system. Another example of a requirement for a pulse advanced in time with respect to the input synchronizing reference is that required to start the reference ramp in the phase detector in the horizontal scanner loop.

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The timing references must be carefully spaced with respect to each other to reflect the delays of the lowpass elements used in the machine and the slopes of the ramps used in various phase detectors. In many prior-art designs, this has been done through the use of precision monostable-multivibrator pulse-advancer circuits. These require individual adjustment and careful design against susceptibility to temperature changes. It was therefore determined early in the program that the required array of timing references would be derived digitally through the use of a high-frequency "clock" phase-locked to the horizontal component of the input synchronizing reference. Through the use of a series of dividers and selector gates, and with appropriate reset means for the dividers, it is possible to derive a wide variety of timing pulses separated by an integral number of clock-pulse intervals.

While monostable multivibrators do exist in the system, they are utilized only for such purposes as adjusting the nominal length of reset pulses or the elimination of alternate field pulses, etc.; none of them is critical as regards length of delay produced nor has adjustment means.

Once the digital approach had been decided upon, a number of other possibilities opened up. The most important is that of moving the entire coordinated array of output timing references in time with respect to the input synchronizing reference, in order to accommodate system cable delays and to adjust the machine timing as required for editing purposes with the additional facility of holding the established time advance (or delay) in a very stable manner through the use of a digital delay system incorporating latch circuits. Both the adjustment for cable delay and the editing aspects of the overall timing adjustment will be discussed further below.

The overall timing adjustment is in increments corresponding to the clock-pulse interval, with an overall range of approximately ±1 horizontal line. In any ordinary system this range is, of course, far greater than required, but the system implementation made it convenient to provide such a range.

System Implementation and Design Choices

In Fig. 1 we have a simplified block diagram of the basic reference-generation system. The heart of the system might be said to be the phase-locked loop which accepts the horizontal input

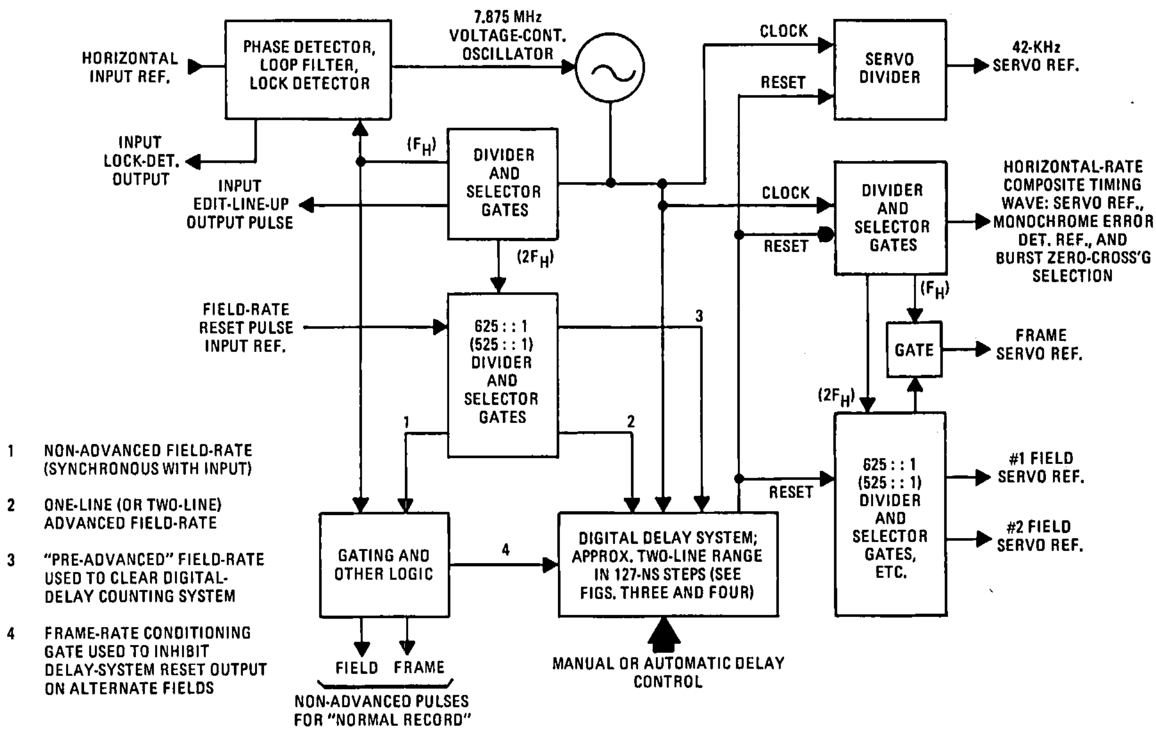

Fig. 1. Simplified block diagram of basic reference generation system.

reference. After appropriate division from the 7.875-MHz clock oscillator, the divider system produces a number of outputs including one at the horizontal rate to which the input reference is compared. The choice of the oscillator frequency was based on these considerations:

(1) The clock-pulse interval had to be short enough to be comfortably less than the duration of one color-subcarrier cycle, such that in system line-up we could accommodate final color phasing with a system-phase control having a range of one cycle; and

(2) for favorable commonality between the CCIR and NTSC versions of the machine, the frequency chosen should be at, or near, an integral multiple of the horizontal scanning rate for each system.

The frequency chosen represents 504 times the CCIR horizontal rate and 500 times 15.75 kHz; a slight readjustment of the free-running rate of the voltage-controlled oscillator is necessary to accommodate the NTSC horizontal frequency.

The phase-locked loop in question has a static phase error which is nominally 15 ns and a maximum of 25 ns over the environmental range to be expected. Both the horizontal input reference and the field-rate input reference are derived from an input reference selector/conditioner system which will be described later.

An output of the loop/divider system occurring at twice horizontal frequency is applied to a counter chain very similar to those used in an ordinary television synchronizing generator. An exception is that in addition to the output labeled "1" which is nominally synchronous with the input field-rate signal, additional outputs labeled "2" and "3" are derived from selector gates within the system which are advanced in time with respect to the input.

A very important point to be noted is that the field-rate reset pulse is applied in such a way that it occurs midway between two of the driver input pulses. Once the divider has been reset appropriately, subsequent field-rate reset pulses do not affect the timing of the outputs, or could be considered redundant, provided they do not shift by more than one-quarter of a horizontal line time for their nominal position midway between input pulses. This margin tends to provide good immunity against the effects of noise on the vertical separator which provides the reset pulse, and assures that the field-rate outputs of the divider system are accurately timed to the master-clock-pulse edges and not to the separated vertical pulses.

The output of the divider system labeled "2" is advanced either one or two lines with respect to the synchronous output labeled "1." In the IVC-9000, a dropout compensator system may be optionally employed which includes a one-line signal delay. In the event the dropout compensator option is not employed, connections associated with the jumper board, which replaces the dropout compensator, cause output "2" to be advanced by only one line rather than two.

Output "2" is applied to a digital delay system which consists essentially of a 10-bit counter clocked by the 7.875-MHz voltage-controlled oscillator and followed by a 10-bit digital comparator. The comparator output is at the field rate, but additional logic in the form of the frame-rate conditioning gate output labeled "4" causes the master reset pulse to occur at the frame rate. Just prior to each counting operation, the pre-advanced pulse labeled "3" is used to clear the counter to zero; this pulse occurs approximately $12\frac{1}{2}$ lines prior to counter enabling. In all cases, the count at which reset occurs is determined by a 10-bit parallel input to the digital comparator which is derived from a series of toggle switches in the case of normal-play operation and the count stored in latches in the case of edit operations. These situations will be discussed in greater detail below.

The master reset pulse thus derived is applied to another series of divider and selector gates very similar to those previously described. Since the digital delay system has a two-line range, we can thus advance or delay the outputs of the second divider system by one line with respect to the input reference. The horizontal-rate output timing wave is made up as a composite signal having three significant transitions:

(1) one which starts the reference ramp of the horizontal scanner servo phase detector;

(2) one which starts the reference ramp for the monochrome error detector; and

(3) a transition which occurs at or near the center of the reproduced color burst for zero-crossing selection.

It should be noted that the three significant transitions of the composite wave just described are spaced by an integral number of clock-pulse intervals, and that this spacing is held invariant as the entire array of pulses is moved in time through the shifting of the timing of the master reset pulse.

Through the use of another divider chain and associated selector gates, various outputs to the servo system for frame and field reference pulses are provided.

In addition to the outputs already mentioned, a 42-kHz reference wave is provided at the output of the servo divider. It is this wave which establishes the basic rotational rates of the scanner and capstan systems except, of course, when the capstan is driven at shuttling speeds. The utilization of this servo reference wave will be described more fully in the following paper.

In normal record operations, field and frame references synchronous with the input reference are required, as shown in the lower lefthand corner of the Figure. The representation is made in this fashion for clarity; in the actual implementation of the system gating arrangements are employed such that the outputs at the righthand side of the Figure are made synchronous with the input by, in effect, utilizing the non-advanced field-rate pulse labeled "1" as the master reset.

Also, in the interest of clarity, several additional features of the reference-generation system have been omitted from the Figure. These include gating means to provide the 12.5-Hz color-frame signal used in the capstan servo system . . . this is essential for proper color edits in the PAL and SECAM systems. In the NTSC systems, 15-Hz pulses are derived for capstan lockup. Presently these are of arbitrary phase, but when the SMPTE or some other body firmly establishes the relationship between the deflection-sync and subcarrier components of the composite wave, it will be relatively easy to convert the IVC-9000 to a system employing automatic NTSC color framing. No provision has been made for full color framing in PAL, that is to say with due attention to the relative phase of the subcarrier. Aside from being unbearably complicated this involves an 8-field sequence which tends to unduly constrict the editor's choices as to the point of edit, as well as introducing the possibility of an unduly lengthy capstan lockup sequence.

Input Reference Conditioning

Before considering the digital delay system in its several modes of operation, we will examine the input reference selector/conditioner block diagram of Fig. 2. It is from this block that the horizontal and field-rate pulses are derived from the input synchronizing reference. At the upper lefthand corner of the Figure we have stripped composite sync from the video input system. This sync has experienced delays, not only due to the signal lowpass filter but also that of a chroma-elimination filter utilized in the sync stripper proper. The total delay is of the order of a microsecond and is of no particular consequence; but, under the assumption that usually composite station sync will arrive at the machine in exact synchronism with the composite video signal, a filter having equivalent delay is provided at the station-sync input shown immediately below before the two signals are applied to the selector.

Separate toggle switches are provided

(on the PC board) for selection of the sync source to be utilized in record and normal-play modes. These are shown in the positions which would probably be most commonly employed, with stripped sync being used in record and edit modes and station sync being used in normal playback.

Since accidents do happen, we have also provided a detector for the presence of station sync and a gating arrangement whereby the selector system automatically reverts to stripped sync if station sync is missing.

The selector system is followed by a one-shot which eliminates equalizing pulses and alternate vertical serrations and by a vertical sync separator. These blocks provide the useful output references mentioned above. Referring back to Fig. 1, we notice in the upper lefthand corner a lock detector output associated with the phase-locked loop. This is the output of a carefully-designed circuit which indicates "no lock" not only in the event of loss of the horizontal input reference but also if extraneous pulses occur outside a narrow window which coincides with the reference ramp used in the loop phase detector. Thus, if noise is applied to the input of the system, such as might occur if one were dubbing and ran beyond the recorded material on the tape from which the dub was being taken, a "no lock" output indication would occur.

Not shown in Fig. 1 is a crystal-controlled oscillator system which effectively replaces the voltage-controlled oscillator whenever a "no-lock" condition exists. This has associated with it a separate divider, also not shown, such that the one associated with the phase-locked loop can continue to monitor the input to see if lock can be re-established. Thus the full array of output signals is constantly available even under "no lock" conditions.

Referring once more to Fig. 2, we note that the lock detector output is also used to inhibit the field-rate reset pulse under "no lock" conditions. As mentioned before, resetting of the 625:1 (or 525:1) divider is essentially a redundant operation once the phase has initially been established. By locking out the reset pulses under "no lock" conditions, we thus continue to have a full array of field, frame, and horizontal-rate output pulses which will not be disturbed even if the input to the machine is merely noise. Thus, none of the servo systems is disturbed such as to cause mishandling of the tape or other problems in the event that the machine input is suddenly missing or reverts to noise.

The frequency of the crystal-controlled oscillator is sufficiently accurate and stable that through the medium of a phase-locked loop system, which produces a subcarrier corresponding to the average phase of the off-tape burst, fully

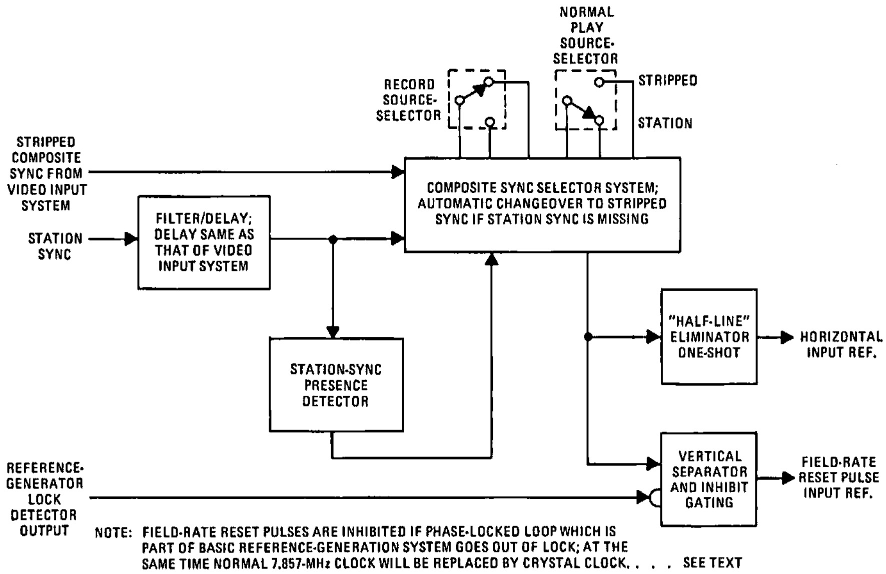

Fig. 2. Simplified block diagram of input reference selector/conditioner.

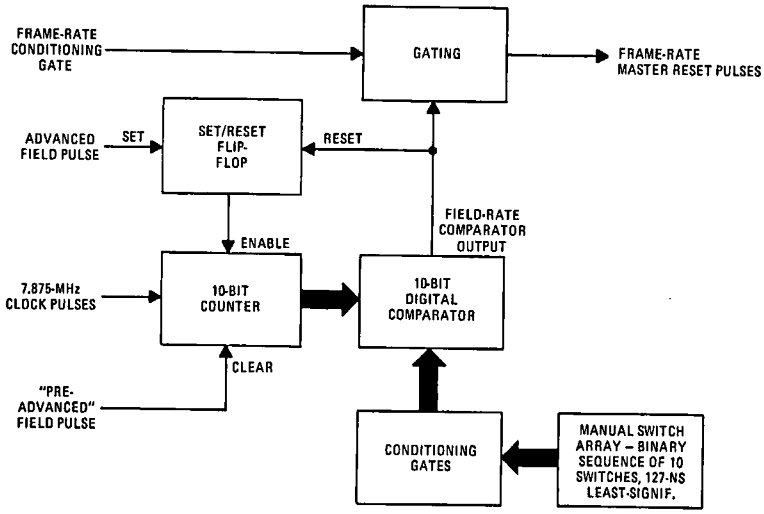

Fig. 3. Simplified block diagram of digital delay system — normal-play mode.

color-corrected video suitable for viewing on an internally-synchronized monitor can be provided even when no inputs of any kind are provided to the machine. This feature is considered potentially useful in mobile and remote applications in which "quick look" playback may be desired but when no machine inputs are available.

System Timing in Normal Playback

Referring now to Fig. 3, we have a representation of the digital delay system in the normal-play mode. Approximately $12\frac{1}{2}$ horizontal lines prior to each counting operation the pre-advanced field pulse clears the 10-bit counter to zero. When the one-line or two-line advanced field pulse arrives to set the flip-flop, counting is enabled and continues until it equals that programed into the 10-bit digital comparator. At this point the comparator output resets the flip-flop to cause counting to cease. The comparator output is also applied to a simple gating system which eliminates alternate output pulses and thus provides the frame-rate master reset pulses.

In the normal-play mode of operation, programing of the digital comparator is accomplished by an array of toggle switches located on one of the PC cards. Once set to accommodate the particular cable and distribution-amplifier delays encountered in any given installation, these do not again require adjustment. The conditioning gates shown in this figure actually comprise a set of ten two-by-one switches which are used to cause the digital comparator to use the output of latches as an input, rather than the manual switches in edit modes, as will be described below.

Edit Line-up

For an edit involving minimal timing discontinuity at the point of edit, it is necessary that if we are 50% down on the leading edge of horizontal sync (a convenient timing reference point chosen for illustrative purposes) in the edit-play mode in the RF at the video head, then

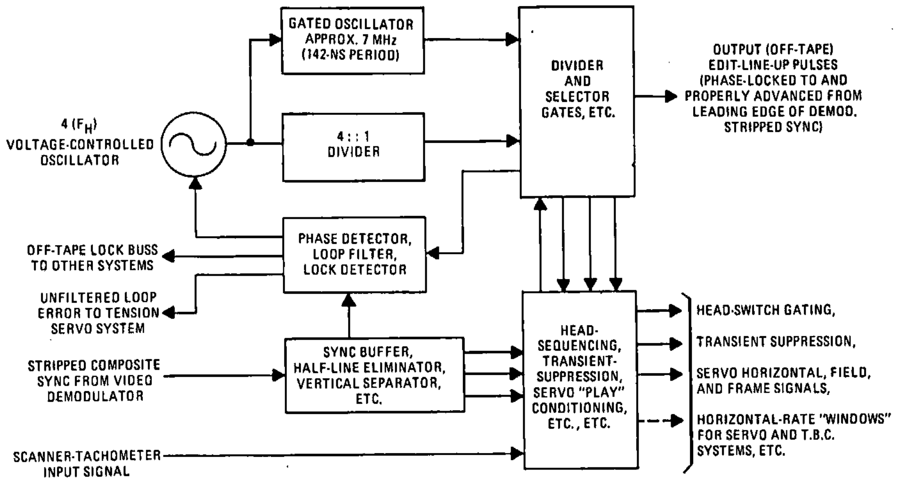

Fig. 4. Simplified block diagram of off-tape sync processor.

the modulated RF about to be recorded at the video head should be timed exactly to correspond to this timing reference point.

Due to certain inevitable geometrical tolerances in the system such as tachometer-disc position in the scanner, and particularly under tape-interchange conditions, we cannot be sure that the above-mentioned condition will be met. Fortunately, the time delays associated with the RF and video circuitry do not vary. If we can derive a pulse representing the leading edge of horizontal sync from the input about to be recorded, and another representing the leading edge of horizontal sync in demodulated reproduced video, with the proper delay established between the two to accommodate the invariant electrical delays of the system, we can, by causing these pulses to coincide in time, achieve the desired edit line-up at the video head. Again referring to Fig. 1, we note the input edit line output pulse shown derived from the divider and selector gates of the phase-locked loop. In the implementation of the line-up system, we have chosen to use an input reference pulse which is substantially synchronous with the leading edge of the horizontal input reference and to advance the pulse derived from the reproduced or off-tape video. It will be appreciated that we could as well have delayed the input line-up pulse and used an off-tape line-up pulse synchronous with the leading edge of sync of the reproduced video.

Off-Tape Edit Reference Derivation

The off-tape sync processor shown in Fig. 4 performs a variety of functions as is indicated by the relatively large number of outputs shown, but in the following discussion we will confine ourselves to its use in the edit line-up scheme. The horizontal component of stripped composite sync from the video demodulator, after processing in the sync buffer, half-line eliminator, etc., is applied to a phase-locked loop system which utilizes a voltage-controlled oscillator operating at four times the horizontal rate. At each transition of the oscillator output, a gated oscillator operating at approximately 7 MHz is applied to a divider and selector gate system. One of the outputs, after proper conditioning by an auxiliary 4:1 divider, starts the ramp in the phase detector used in this phase-locked loop. From selector gates connected to the divider for the 7-MHz gated oscillator we obtain a wide variety of pulses whose widths and spacings correspond to integral numbers of gated-oscillator cycles, or integral multiples of the 142-ns period of the gated oscillator. Since the gated oscillator operates on a start-stop basis, extreme accuracy of its free-running frequency is not essential. In other words, since it starts afresh for each horizontal sampling interval, cumulative errors are not possible.

The phase-locked loop described is a nominal static phase error of approximately 50 ns, with a maximum error of 70 ns under worst-case environmental conditions. Loop bandwidth is such that the output edit line-up pulse does not reflect minor short-term timing variations which might be occasioned by a moderate amount of noise in the reproduced stripped composite sync. Gating is such that when the line-up pulse is timed coincident with the input edit line-up previously described, edit line-up at the video head will be correct.

Input Edit Reference Derivation; Edit Line-up Action

Figure 5 is a representation of the digital delay system in the edit modes. In edit play, the input and output line-up pulses previously described are applied to a phase detector and loop filter. The filtered output error voltage is applied to a voltage-controlled one-shot which is triggered by the advanced field pulse. The 10-bit counter, which is the same one as was described for the normal-play mode (but with some additional gating implied), counts for an interval which corresponds to the length of the output pulse of the voltage-controlled one-shot. At the end of the one-shot output pulse, counting is disabled and counter contents are strobed into an array of latches which thus carry, in terms of the number of 7.875-MHz clock-pulse intervals attained, a representation of the output pulse length of the voltage-controlled one-shot. The counter is cleared by the pre-advanced field pulse discussed in connection with the normal-play mode of operation.

In the edit-play mode the termination of the output pulse of the voltage-controlled one-shot also provides, via gating which eliminates alternate pulses, the frame-rate master reset pulses. Thus, as the length of the one-shot pulse is varied, the timing of the entire array of output pulses of the reference-generation system, and hence that of the output of the VTR relative to the input reference synchronizing signal, is varied.

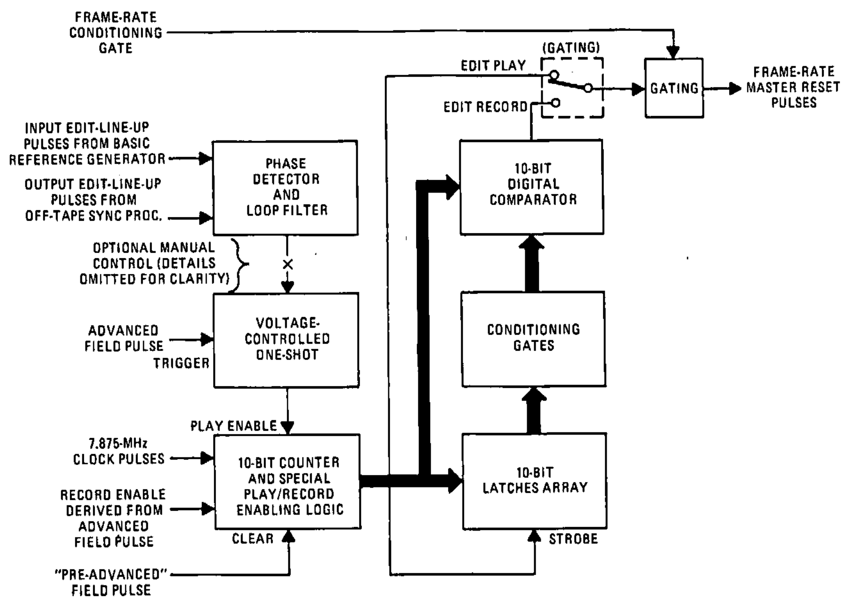

Fig. 5. Simplified block diagram of digital delay system — edit modes.

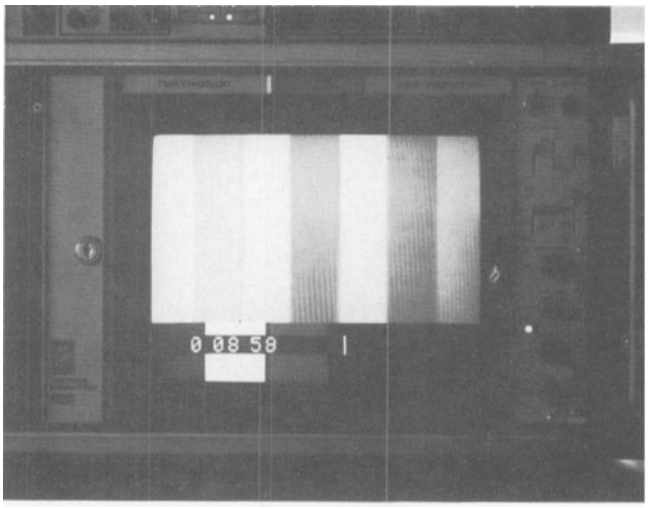

Fig. 6. Bridge monitor display — before edit line-up.

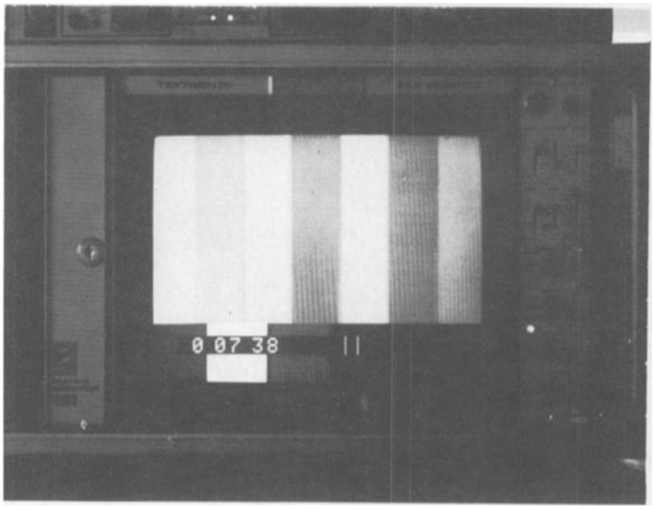

Fig. 7. Bridge monitor display — edit line-up achieved.

It was mentioned earlier that one-shots were used in this system only for alternate-pulse elimination and similar noncritical applications. At least in the automatic mode of operation, the one-shot we have been discussing may also be considered noncritical as to environmental influences since it is operating within a closed-loop system. If its output pulse length is incorrect then the input and output edit line-up pulses will no longer coincide, and an error voltage will be produced to correct the pulse length, and hence machine timing, to cause them to coincide.

When we go from edit play to edit record, gating means within the counter system will cause it to be cleared by the pre-advanced and subsequently enabled by the advanced field pulse once each field. When the attained count corresponds to the contents of the latches, an output will be provided from the digital comparator which, after appropriate gating, forms the frame-rate master reset pulse. Thus to a tolerance of one-count pulse (or 127 ns) the timing which was established in edit play will be maintained in edit record.

Line-up Display and Other Features

In Fig. 6 we have a representation of the bridge monitor display in which the tape-timer mask has been expanded to include an area in which pulses representing the input and output edit line-up pulses form vertical white lines. Incidentally, for various technical reasons, the pulses displayed are not those which are applied to the edit line-up phase detector, but the representation is quite accurate since they are related to them by fixed numbers of clock-pulse intervals in each case. When these vertical lines are made to coincide (see Fig. 7) we are assured that edit line-up has been achieved. Again referring to Fig. 5, there is an optional manual system for achieving edit line-up. Quite frankly, this optional manual system is present because early in the program we were not sure that the automatic system would operate properly. We must bear in mind that we have here a rather enormous closed loop, since we are moving the entire videotape recorder back and forth in time with respect to its input references.

Not shown in Fig. 5 is a manual "freeze" switch which can cause the contents of the latches to remain fixed, once established either automatically or manually in the edit-play mode. This "freeze" switch is needed because it takes a finite time for the machine to stabilize in all its functions when going from edit record to edit play, and it is possible that if an extremely rapid succession of inserts were attempted, with very brief edit-play intervals, an erroneous line-up might occur. Because the line-up system is intended to accommodate geometrical interchange factors and long-term environmental factors, freezing of the latches contents in this application has no particular disadvantage. It is only necessary to provide an adequate long edit-play interval (which amounts to only a few seconds) before "freezing" to prepare the machine for a rapid series of successive insert edits.

It should be noted that because the edit line-up timing is established digitally, that is to say without the use of a capacitive store or other elements susceptible to environmental influences, quite long inserts can be accommodated with the assurance of a proper exit.

Other "Freeze" Functions; Conclusion

In this same context, the IVC-9000 contains two other "freeze" functions:

(1) In edit play, full horizontal scanner lock is attained through the medium of altering the timing of reference scanner tachometer pulses in a digital delay system similar to that previously described. The delay thus established is "frozen" automatically when the edit record mode is entered, and can also be "frozen" by the manual "freeze" switch previously mentioned.

(2) The error signal applied to the vacuum modulator, which is utilized in the automatic tension servo, is also conditioned by a digital system which is capable of being "frozen" in a manner analogous to that described for the edit line-up and horizontal systems.

The horizontal and tension-error memory systems are described more fully in the paper about the servo system by Morgan, immediately following.

In conclusion, it can be stated that the automatic systems just described lead to a VTR in which editing can be performed without the need for the operator to manipulate controls and/or monitor error signals in order to avoid timing discrepancies at the point of edit, a simplification in operational use not known to the author to be present in previously available videotape recorders.

Acknowledgments: While the author was responsible for much of the conceptual approach to the timing system just described, he wishes to gratefully acknowledge the contributions of Nikola Vidovic who, aided by William Moore, performed the detailed implementation of the system.