6.2 Picture signal level

The signal level throughout the active picture period shall correspond to blanking or black level (0 IRE or 7.5 IRE ± 2.5 IRE, respectively (see note 1).

6.3 Signal amplitude

The amplitude of the synchronizing pulses shall be 286 mV + 100 mV – 50 mV. The peak-to-peak amplitude of the subcarrier burst shall be nominally equal in amplitude to that of the synchronizing pulse.

6.4 Rise and fall time of horizontal synchronizing pulses

The rise and fall time of the horizontal synchronizing pulses shall be 140 ns ± 20 ns, measured between the 10% and 90% amplitude levels.

6.5 Jitter

The timing of individual leading edges of horizontal synchronizing pulses shall be within ± 2.5 ns of the timing of leading edges, as averaged over at least one field (see notes 2 and 3).

7 Digital representation

Where equipment will be operated primarily in a digital environment, a serial or parallel representation of a color black or other color video signal may be used as an additional or alternate reference. The digital signal need not conform to 6.2, as APL does not affect sync detection in a digital signal. Reference signals shall conform to appropriate SMPTE standards or recommended practices for digital interface of television signals. Where a composite digital signal is used, a 10-bit representation is recommended.

NOTES

1 Reference signals of higher constant APL are specifically not recommended because they may cause performance degradation related to APL variations between the vertical interval and other parts of the signal. Furthermore, reference signals with changing APL, such as moving video or switched test signals, are also specifically not recommended because they may cause disturbances to the video signal being processed by the equipment for which they are the reference.

2 In order to achieve the level of performance specified, it may be necessary to provide a synchronizing pulse generator to serve the local area. In the presence of hum and noise, it may also be necessary to take steps in the system design to prevent the reduction of the level of performance from that required.

3 Reference signals with less jitter are preferred for many applications. Usually, this is accomplished using a burst-referenced genlock since the burst has less jitter (as per SMPTE 170M) and provides more data for the locking oscillator. Horizontal synchronizing pulses with jitter of less than ± 1 ns may also be useful.

PROPOSED SMPTE STANDARD

SMPTE 267M
Revision of
ANSI/SMPTE 267M-1994

for Television —

Bit-Parallel Digital Interface — Component Video Signal 4:2:2 16×9 Aspect Ratio

Table of contents

1 Scope

This standard defines an interface for system M (525/59.94) wide screen, 16×9 aspect ratio, digital television equipment based on ITU-R 601-2. Two luminance sampling rates are provided, 13.5-MHz sampling providing full-signal compatibility with equipment operating in compliance with ANSI/SMPTE 125M, and 18-MHz sampling providing equivalent horizontal resolution for the 16×9 aspect ratio of this standard as compared to the 4×3 aspect ratio of ANSI/SMPTE 125M. Use of the 18-MHz sampling method also provides 16×9 to the 4×3 aspect ratio translation by sample selection rather than sample interpolation as would be required with 13.5-MHz sampling. The standard has application in the television studio over distances up to 300 m (1000 ft) for 13.5-MHz sampling and 225 m (750 ft) for 18-MHz sampling.

2 Interface characteristics

2.1 The video signal is transmitted in the form of one luminance (Y) and two color-difference components (scaled version of R–Y and B–Y).

2.2 The video signal is transmitted at the 4:2:2 family level of ITU-R 601-2, with a nominal luminance sampling frequency of 13.5 MHz or 18 MHz. Provision is made to convey signals at 10-bit precision. Because of the potential use of 8-bit data, all synchronizing signals (EAV, SAV, ANC) must be detected by reference to the eight most significant bits only.

2.3 The bits of the digital code words that describe the video signal are transmitted in a parallel arrangement using 10 conductor pairs as described in 6.2.2. Each pair carries a multiplexed stream of bits (of the same significance) of each of the component signals. Accordingly, the bit rate used in each pair is nominally 27 Mbits/s for 13.5-MHz sampling and 36 Mbits/s for 18-MHz sampling. An eleventh conductor pair carries a clock signal at 27 MHz or 36 MHz, respectively.

2.4 The signals on the interface are transmitted using balanced conductor pairs for a distance up to 50 m (160 ft) for 13.5-MHz sampling and 40 m (120 ft) for 18-MHz sampling without equalization, and up to 300 m (1000 ft) for 13.5-MHz sampling and 225 m (750 ft) for 18-MHz sampling with appropriate equalization.

2.5 The interface consists of one transmitter and one receiver in a point-to-point connection.

2.6 Parameters of the signal format are chosen to facilitate conversion to and from a serial digital interface format. The serial digital interface defined in SMPTE 259M is the preferred method for the interconnection of digital equipment when cable lengths exceed 50 m.

2.7 The interface allows the transmission of appropriate ancillary signals that may be multiplexed into the data stream during video blanking intervals.

2.8 Where hexadecimal values are used, they are indicated by a subscript h, such as $3FF_h$; other values are decimal.

3 General

3.1 Signal convention

The signaling sense of the voltage appearing across the interconnection cable is positive binary and defined as follows (refer to figure 1):

3.1.1 The A terminal of the transmitter shall be negative with respect to the B terminal for a binary 0 (LOW or L or OFF) state.

3.1.2 The A terminal of the transmitter shall be positive with respect to the B terminal for a binary 1 (HIGH or H or ON) state.

3.2 Signal names

The data lines are designated DATA 0 through DATA 9. The group of 10 signals is identified by placing parentheses around the range of subscripts included, as DATA (0-9). When 8-bit signals are conveyed by the interface, DATA (2-9) shall be used and DATA (0-1) shall be set to zero. DATA 9 is always the most significant bit.

3.3 Component coding considerations

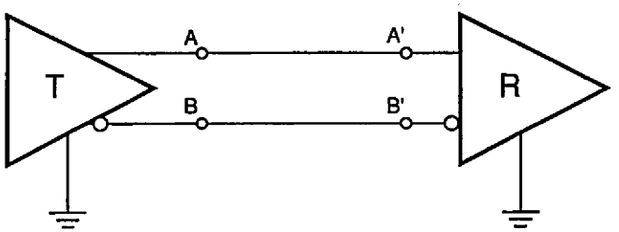
Spectral characteristics of analog signals to be encoded must be restricted to eliminate aliasing. Filters, as described in ITU-R 601-2, annex III, may be considered for use with 13.5-MHz sampling and can be scaled for 18-MHz sampling. Designers are cautioned to use filter characteristics that are best suited for their particular product application.

3.4 Sin x/x considerations

The characteristics of the data word at the interface are based on the assumption that the location of any required sin x/x correction is at the point where the digital signal is converted to an analog format.

3.5 Blanking interval considerations

This standard does not require the device feeding the interface to transmit video data during the entire blanking interval. Therefore, ancillary information may be inserted into the horizontal blanking interval by the user within the constraints specified in 4.4 and 4.5.



T = transmitter
R = receiver
A,A' = the data line
B,B' = the return line

Figure 1 – Positive binary signal convention

The vertical blanking duration is a minimum of nine lines. Ancillary information may be inserted into this nine-line interval by the user within the constraints specified in 4.4 and 4.5.

3.6 Signal specifications

All digital signal time intervals are specified at the half-amplitude points. All transitions are specified between the 20% and 80% amplitude points.

3.7 Electromagnetic interference considerations

Digital apparatus can radiate a significant amount of energy at harmonics of the clock frequency. In the case of 13.5-MHz sampling, clock harmonics lie at 121.5 MHz and 243 MHz, both of which are aeronautical distress frequencies. Equipment and system designers must, therefore, pay particular attention to the provision of adequate shielding.

3.8 Document of compliance

It is suggested that any documentation indicating compliance with this standard be written in such a manner that use of 13.5-MHz and/or 18-MHz sampling is clearly defined. This can be accomplished with a suffix to the numerical designation such as SMPTE 267M-13.5 or SMPTE 267M-18.

4 Interface format

4.1 General description

The interface consists of a unidirectional, 11-pair interconnection between a transmitting equipment and a receiving equipment. Video data, timing reference information, and ancillary signals are time multiplexed and transferred on 10 data pairs in NRZ form. An eleventh pair provides a synchronous clock.

4.2 Encoding parameters

Table 1 summarizes the encoding parameter values.

4.3 Interface characteristics

Table 2 specifies the interface characteristics.

4.4 Digital blanking relationship

4.4.1 Horizontal sync relationship — 13.5-MHz sampling

Figure 2a shows the relationship between video signals in the digital and analog domains for 525-line systems. Figure 2b shows the multiplex structure.

Transmitted during each active line are 1440 multiplexed luminance and chrominance values (720 luminance, 360 chrominance C_R, and 360 chrominance C_B values).

Eight of the remaining 276 interface clock intervals are used to transmit synchronizing information; the other 268 interface clock intervals may be used to carry ancillary information.

The first of these 1716 interface clock intervals is designated line word 0 for the purpose of reference only. The 1716 sample words per total line are therefore numbered 0 through 1715. Intervals 0 through 1439, inclusive, contain video data. The interface clock intervals occurring during digital blanking are designated 1440 through 1715.

Intervals 1440 through 1443 are reserved for the end-of-active-video (EAV) timing reference described in 4.5.3. Intervals 1712 through 1715 are reserved for the start-of-active-video (SAV) timing reference described in 4.5.3.

The half-amplitude point of the leading (falling) edge of the analog horizontal sync signal shall be coincident with a sample point which would be conveyed by word 1473 if carried across the interface.

4.4.2 Horizontal sync relationship — 18-MHz sampling

Figure 2c shows the relationship between video signals in the digital and analog domains for 525-line systems. Figure 2d shows the multiplex structure.

Transmitted during each active line are 1920 multiplexed luminance and chrominance values (960 luminance, 480 chrominance C_R, and 480 chrominance C_B values).

Eight of the remaining 368 interface clock intervals are used to transmit synchronizing information; the other 360 interface clock intervals may be used to carry ancillary information.

Table 1 – Encoding parameters

Coded signals: These values are obtained from the gamma precorrected signals	$Y = 0.299R + 0.587G + 0.114B$ $C_R = 0.713 (R–Y) = 0.500R – 0.419G – 0.081B$ $C_B = 0.564 (B–Y) = 0.500B – 0.169R – 0.331G$			
Number of samples per line:	13.5-MHz sampling		18-MHz sampling	
	Total	Active	Total	Active
– luminance (Y)	858	720	1144	960
– each color-difference signal (C_R, C_B)	429	360	572	480
– total number of samples	1716	1440	2288	1920
Sampling structure:	Orthogonal: line, field, and frame repetitive; C_R and C_B samples are cosited with odd (1st, 3rd, 5th) samples in each line			
Sampling frequency:	13.5-MHz sampling		18-MHz sampling	
– luminance (Y)	13.5-MHz nominal		18-MHz nominal	
– each color-difference signal (C_R, C_B)	6.75-MHz nominal		9-MHz nominal	
Form of encoding:	Uniformly quantized, PCM, 10 bits per sample, for the luminance and each color-difference signal.			
Correspondence between video signal levels and quantization levels:				
– luminance (Y)	877 quantization levels with the black level corresponding to level 64 and the peak white level corresponding to level 940.			
– each color-difference signal (C_B, C_R)	897 quantization levels symmetrically distributed about level 512, corresponding to the zero signal.			

Table 2 – Interface characteristics

Digital format	Parallel: 11 balanced signal pairs carrying clock and 10 data bits
Interface clock, 13.5-MHz sampling	27.0 MHz nominal
Interface clock, 18-MHz sampling	36.0 MHz nominal
Voltage levels	Standard ECL (10K or 10KH series)
Driver impedance	Standard ECL (10K or 10KH series)
Receiver impedance	110 ohms nominal, balanced

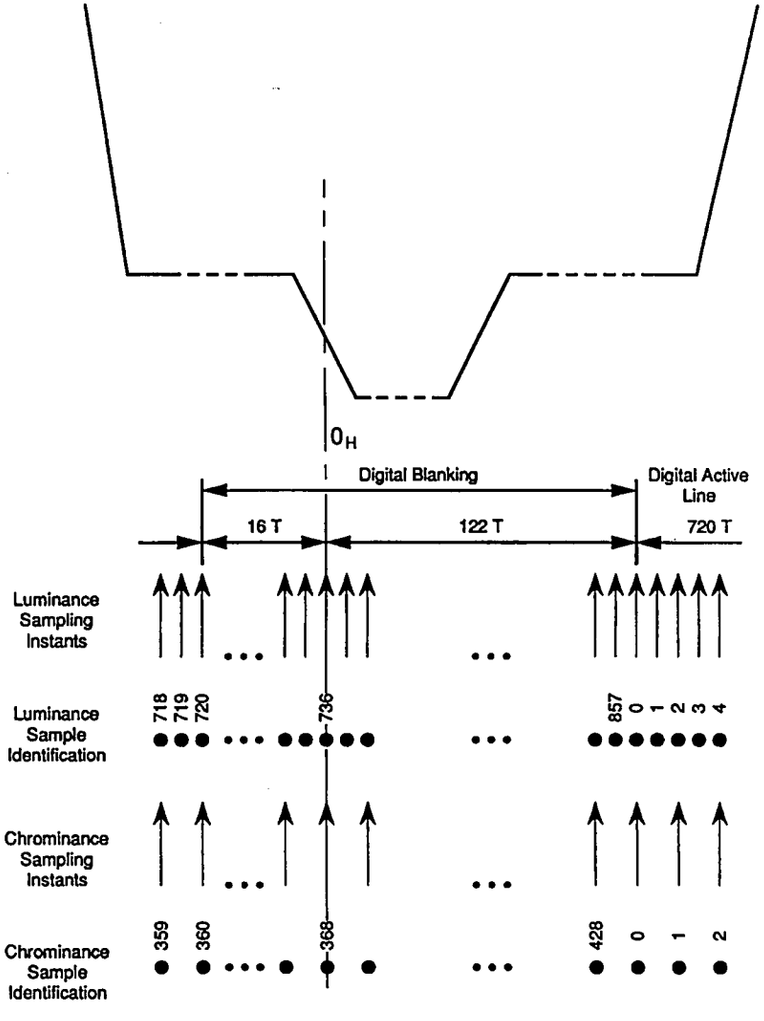


Figure 2a – Horizontal sync relationship — 13.5-MHz sampling

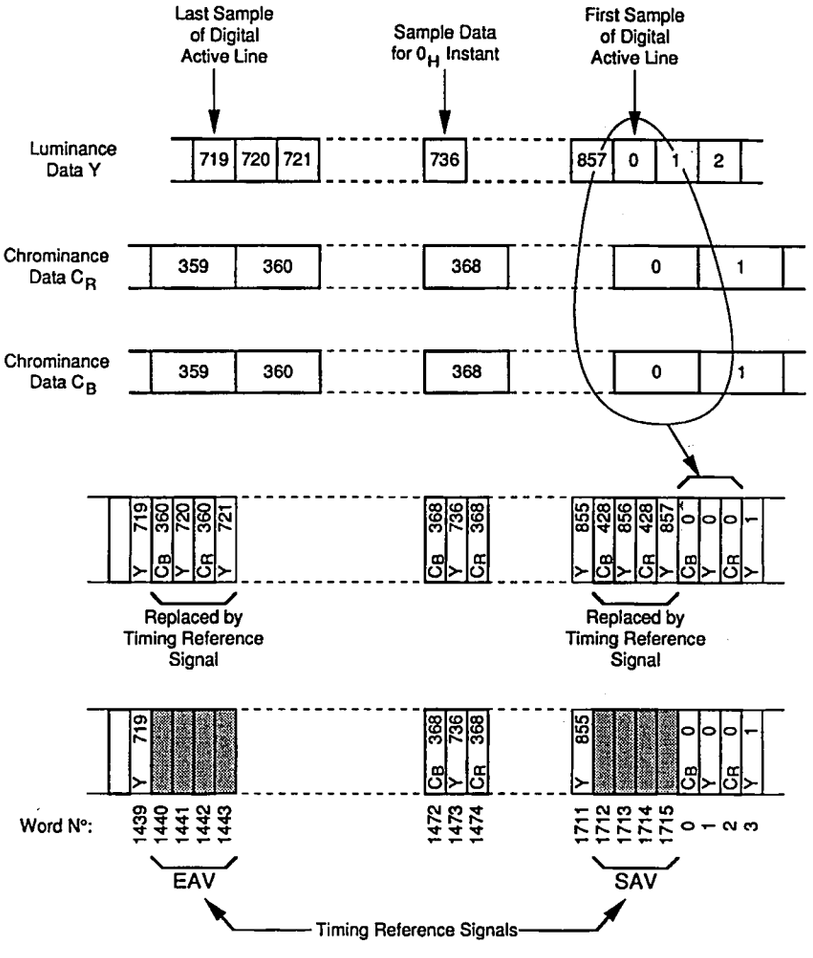


Figure 2b – Multiplex structure — 13.5-MHz sampling

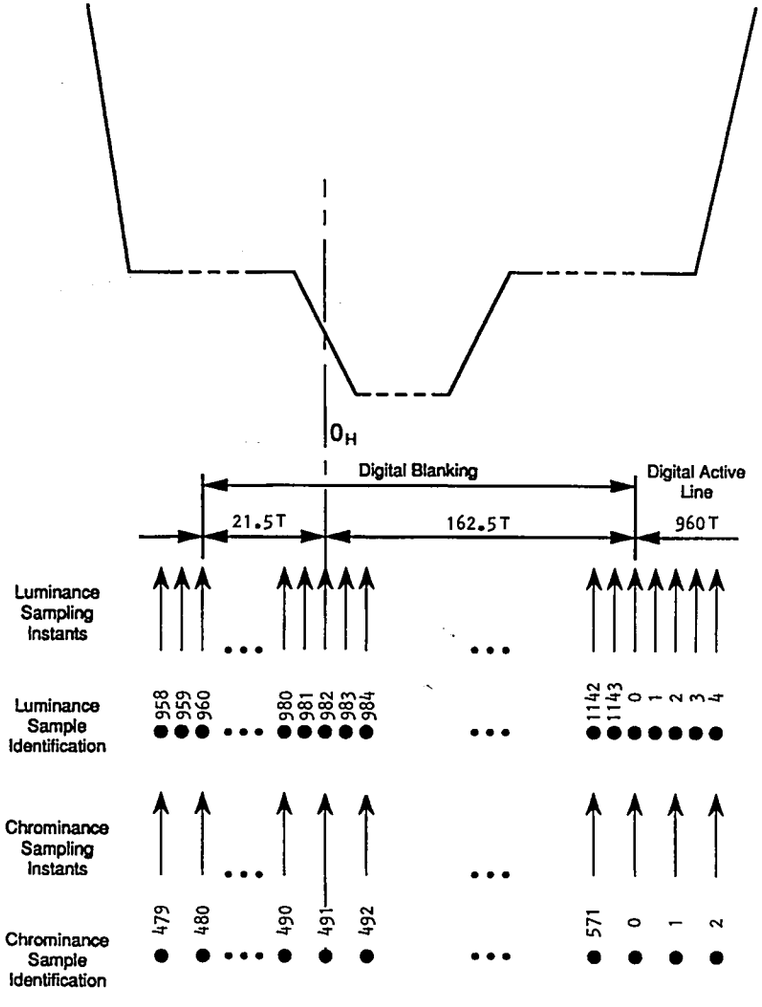


Figure 2c – Horizontal sync relationship — 18-MHz sampling

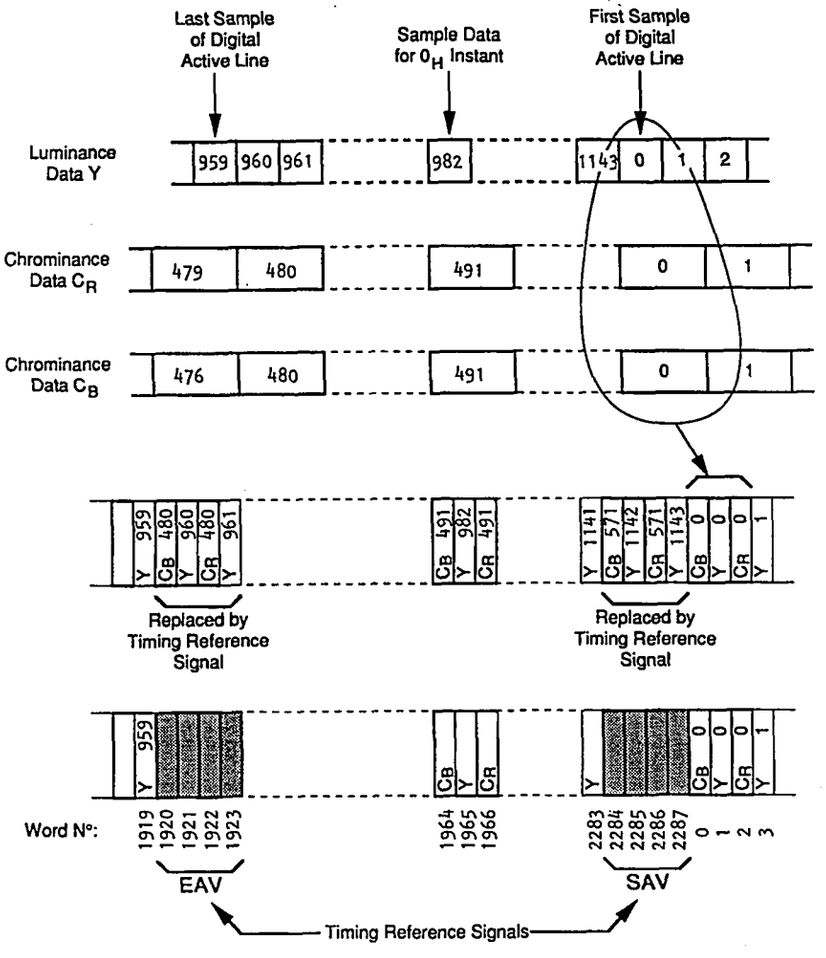


Figure 2d – Multiplex structure — 18-MHz sampling

The first of these 2288 interface clock intervals is designated line word 0 for the purpose of reference only. The 2288 sample words per total line are therefore numbered 0 through 2287. Intervals 0 through 1919, inclusive, contain video data. The interface clock intervals occurring during digital blanking are designated 1920 through 2287.

Intervals 1920 through 1923 are reserved for the end-of-active-video (EAV) timing reference described in 4.5.3. Intervals 2284 through 2287 are reserved for the start-of-active-video (SAV) timing reference described in 4.5.3.

The half-amplitude point of the leading (falling) edge of the analog horizontal sync signal shall be halfway between the sample points which would be conveyed by luminance samples 981 and 982 if carried across the interface. Placement of horizontal sync between the two samples is explained by figure G.1.

4.4.3 Vertical sync relationship

Figure 3 shows the relationship between video signals in the digital and analog domains for 525-line systems.

4.5 Video data signal format

4.5.1 Data signal format

Data is transmitted across the interface on 10 data pairs: DATA 0 through DATA 9. DATA 9 is the most significant bit (MSB). Of the 1024 levels, 1016 are used to express quantized values (digital levels 4 through 1019 or 004_h through $3FB_h$ in the hexadecimal representation) of the 10-bit word.

Data levels 0 to 3 and 1020 to 1023 (000_h to 003_h and $3FC_h$ to $3FF_h$ in the hexadecimal representation) are reserved to indicate timing references.

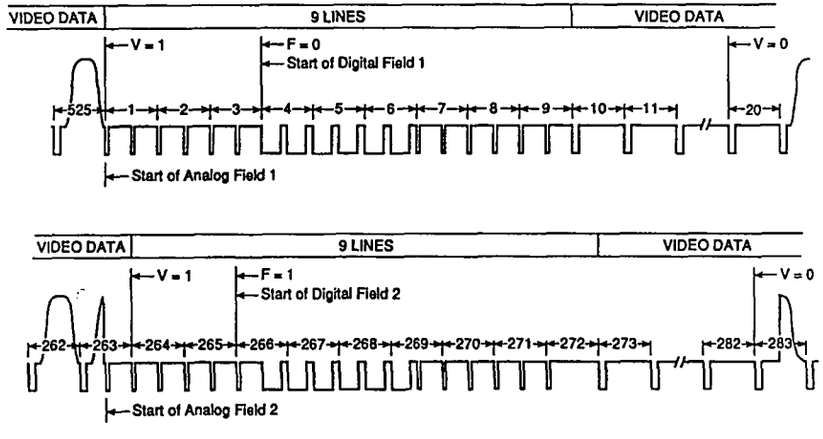


Figure 3 – Relationship of video data/vertical sync

4.5.2 Multiplex structure

The video data words shall be conveyed as a 27 Mword/s multiplex for 13.5-MHz sampling and 36 Mword/s multiplex for 18-MHz in the following order:

C_B Y C_R [Y] C_B...

where the three words C_B Y C_R refer to cosited samples, the following word [Y] being an isolated luminance-only sample. The C_B and C_R samples are cosited with the first and subsequent alternate Y samples (0, 2, 4...) on each line. (See figures 2b and 2d.) The first video data word in each active line period shall be C_B.

4.5.3 Timing reference signals — Video

Figures 2a and 2c show the position of the timing reference signals with respect to horizontal blanking in the multiplexed data stream. It is implicit that the timing reference signals are contiguous with the video data, when present, and continue through the vertical blanking interval.

Each timing reference signal consists of a four-word sequence in the following format:

3FF 000 000 XYZ

Because of the existence of both 8-bit and 10-bit data, for detection purposes all values in the ranges 000_h-003_h and $3FC_h$-$3FF_h$ must be considered equivalent to 000_h and $3FF_h$, respectively.

The first three words are a fixed preamble. The fourth word shall contain information defining:

- even field (field 2) identification;
- state of vertical blanking;
- state of horizontal blanking.

Figure 4 is a spatial representation of the timing reference signals during a television frame. Assignment of bits within the fourth word is shown in table 3. Values for F and V change in the EAV associated with the blanking interval of the line number indicated. P0, P1, P2, and P3 have states dependent on states of bits F, V, and H according to table 4. Lines are numbered from 1 through 525 as shown in figure 3. Vertical blanking in the digital interface is in full-line increments. EAV and SAV are the digital horizontal synchronization signals and occur on every line.

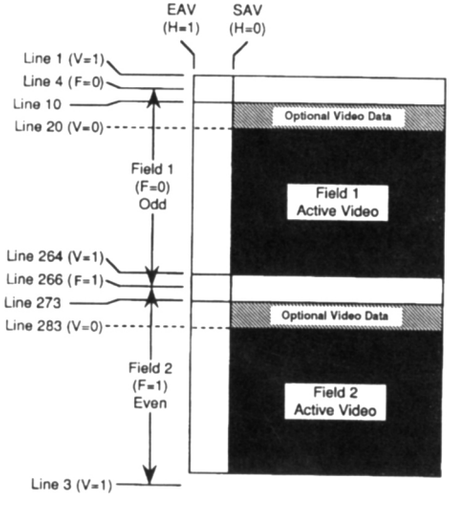


Figure 4 – Timing reference signal locations

Table 3 – Timing reference signals

13.5/18-MHz sampling Bit	Words 1440/1920 and 1712/2284	Words 1441/1921 and 1713/2285	Words 1442/1922 and 1714/2286	Words 1443/1923 and 1715/2287	
9	1	0	0	1	Fixed
8	1	0	0	F	F = 0 during field 1 F = 1 during field 2
7	1	0	0	V	V = 0 during active video V = 1 during vertical blanking
6	1	0	0	H	H = 1 for EAV H = 0 for SAV
5	1	0	0	P3	See table 4
4	1	0	0	P2	
3	1	0	0	P1	
2	1	0	0	P0	
1	1	0	0	0	
0	1	0	0	0	

NOTES
1 Some equipment can only sense the eight most significant bits.
2 The H, V, and F bits (bits 6-8) provide all the necessary information. Bits 2-5 provide error detection and correction information.
3 Each 525-line digital video frame is divided into two fields. Field 1 contains 262 complete horizontal lines. Field 2 contains 263 complete horizontal lines.
4 The protection bits allow correction of all single-bit errors and detection of two-bit errors.

Table 4 – Protection bit states

Bit	9	8	7	6	5	4	3	2	1	0
		F	V	H	P3	P2	P1	P0		
	1	0	0	0	0	0	0	0	0	0
	1	0	0	1	1	1	0	1	0	0
	1	0	1	0	1	0	1	1	0	0
	1	0	1	1	0	1	1	0	0	0
	1	1	0	0	0	1	1	1	0	0
	1	1	0	1	1	0	1	0	0	0
	1	1	1	0	1	1	0	0	0	0
	1	1	1	1	0	0	0	1	0	0

The interval starting at EAV and ending with SAV is the digital horizontal blanking period as shown in figures 2b and 2d.

Small blocks of data, less than 268 words in total length for 13.5-MHz sampling and 360 words in total length for 18-MHz sampling, including the HANC sequence (as described in 4.6.1), can be transmitted within the horizontal blanking period on every line.

Large blocks of data, up to 1440 words in total length for 13.5-MHz sampling and up to 1920 words in total length for 18-MHz sampling, including the VANC sequence, can be transmitted within the interval starting with the end of SAV and terminating with the beginning of EAV on lines 1 through 19 and 264 through 282 only.

Video data will not be present on lines 1-9 and 264-272 and may optionally be present on lines 10-19 and 273-282. Ancillary data could be optionally transmitted in the active portion of these lines.

The words during:

- horizontal blanking period on every line;
- the active portion of lines 1-9 and 264-272;
- the active portion of lines 10-19 and 273-282 (when video data is present)

not used to transmit ancillary data must have the following values:

- the words corresponding to Y samples must have the value 040_h;

- the words corresponding to C_B and C_R samples must have the value 200_h.

4.6 Ancillary data signal format

Ancillary data may be inserted in any portion of the data stream not occupied by timing reference signals or video data (see 4.4.1, 4.4.2, and 4.4.3). Two categories of ancillary data, HANC and VANC, are defined for different portions of the data stream. Note that the three-word header used to identify ancillary data is the same for HANC and VANC.

4.6.1 HANC data

HANC data are permitted in all horizontal intervals, but not in the active portion of lines. HANC data are of 10-bit format, and each block of HANC data is preceded by the three-word ancillary data header 000_h $3FF_h$ $3FF_h$.

Because of the existence of 8-bit data, for detection purposes all values in the ranges 000_h-003_h and $3FC_h$-$3FF_h$ must be considered equivalent to 000_h and $3FF_h$, respectively.

The ancillary data header may occur multiple times during each horizontal blanking period if different blocks of data are transmitted.

All permitted data identification words and data formats will protect the values (000_h to 003_h) and ($3FC_h$ to $3FF_h$).

4.6.2 VANC data

VANC data are permitted only in the active portion of lines 1-13, 15-19, 264-276, and 278-282. (Lines 14 and 277 are reserved for digital vertical interval time code [DVITC] and video index.) VANC data are of 8-bit format, and each block of VANC data is preceded by the three-word ancillary data header 000_h $3FF_h$ $3FF_h$.

Because of the existence of 8-bit data, for detection purposes all values in the ranges 000_h-003_h and $3FC_h$-$3FF_h$ must be considered equivalent to 000_h and $3FF_h$, respectively.

The ancillary data header may occur multiple times during each line period if different blocks of data are transmitted.

All permitted data identification words and data formats will protect the values (000_h to 003_h) and ($3FC_h$ to $3FF_h$).

4.7 Digital vertical interval time code and video index

Digital vertical interval time code (DVITC) and video index, if present, are carried by the data in the active portion of lines 14 and 277.

4.7.1 DVITC

This signal, if present, is carried by the luminance data in the active portion of lines 14 and 277.

4.7.2 Video index

This signal, if present, is carried by the color-difference data in the active portion of lines 14 and 277. A total of 90 8-bit data words is represented serially by DATA(2) of the 720 color-difference samples of the active portion of the line for 13.5-MHz sampling. A total of 90 8-bit data words is represented serially by DATA(2) of the 960 color-difference samples of the active portion of the line for 18-MHz sampling.

The first color-difference word of the active portion of the line (word 0 of the multiplexed signal, normally a C_B sample) represents the least significant bit (bit 0) of video index word 0. The second color-difference word represents bit 1 of the same word, etc. The last color-difference word of the active portion of the line (word 1438 of the multiplexed signal, normally a C_R sample) represents the most significant bit (bit 7) of video index word 89 for 13.5-MHz sampling. The color-difference word 1438 of the active portion of the multiplexed signal (normally a C_R sample) represents the most significant bit (bit 7) of video index word 89 for 18-MHz sampling.

For all samples, a value of 204_h represents a binary one for the appropriate video index bit, and a value of 200_h represents a binary zero for the appropriate video index bit.

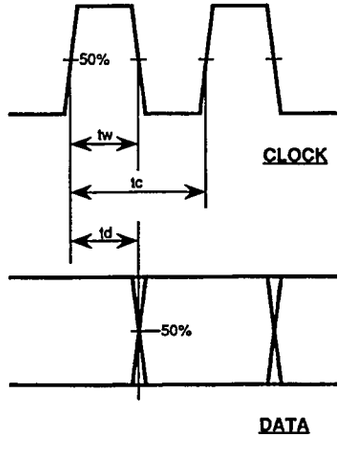
This transmission method ensures that, after digital to analog conversion, the video signal may be sent to an NTSC encoder without any requirement for special blanking. DVITC will be preserved through the encoder without interference from any video index information which may be present.

4.8 Clock signal

4.8.1 Clock signal description (at transmitter)

For 13.5-MHz sampling, the clock signal is a 27-MHz square wave as shown in figure 5. The clock pulse width (tw) is 18.5 ns ± 3 ns.

For 18-MHz sampling, the clock signal is a 36-MHz square wave as shown in figure 5. The clock pulse width (tw) is 13.9 ns ± 2 ns.



Parameter	13.5-MHz sampling	18-MHz sampling
tw	18.5 ns ± 3 ns	13.9 ns ± 2 ns
tc	37.0 ns (nominal)	27.8 ns (nominal)
td	18.5 ns ± 3 ns	13.9 ns ± 2 ns
f_h	15.734 ... kHz (nominal)	

Figure 5 – Clock to data timing (at transmitter)

4.8.2 Clock jitter

For 13.5-MHz sampling, the peak-to-peak jitter between rising edges shall be within 3 ns of the average time of the rising edge computed over at least one field.

For 18-MHz sampling, the peak-to-peak jitter between rising edges shall be within 2 ns of the average time of the rising edge computed over at least one field.

NOTE – Designers of equipment receiving signals from this interface should consider that the jitter requirements for a digital to analog converter may be more restrictive than those of the interface.

4.8.3 Clock data timing relationship

The positive transition of the clock signal nominally occurs midway between data transitions (figure 5).

5 Electrical characteristics

5.1 General

The 11 signals shall be transmitted via balanced signal pairs. Although the use of ECL technology is not specified, the line driver and receiver must be ECL-compatible to permit the use of standard ECL parts for either or both ends in applications where such ECL parts are deemed adequate. (Standard ECL parameters are provided in annex A.)

5.2 Transmitter characteristics

5.2.1 Output impedance

The transmitter shall have a balanced output with a maximum output impedance of 110 ohms.

5.2.2 Common mode voltage

The average of the voltages on the two terminals of the line driver shall be -1.3 V ± 15% with reference to the ground terminal.

5.2.3 Signal amplitude

The generated signal shall lie between 0.8 V peak-to-peak and 2.0 V peak-to-peak, measured across a 110-ohm resistor connected to the output terminals without any transmission line.

5.2.4 Rise and fall times

Rise and fall times shall be no longer than 5 ns and differ by not more than 2 ns, as measured between the 20% and 80% amplitude points across a 110-ohm resistor connected to the output terminals without any transmission line.

5.3 Receiver characteristics

5.3.1 Terminating impedance

The cable shall be terminated by 110 ohms ± 10 ohms.

5.3.2 Maximum input signal

The line receiver must sense properly the binary data when connected directly to a line driver operating at the extreme voltage limits permitted by 5.2.3.

5.3.3 Input sensitivity

The receiver shall require a differential input voltage of no more than 185 mV to correctly attain the intended binary state.

5.3.4 Common mode rejection

The receiver shall operate correctly in the presence of common mode noise having a maximum amplitude of 0.5 V.

5.3.5 Differential delay

The receiver shall operate with a differential delay between the received clock and any received data signals up to 11 ns for 13.5-MHz sampling and 7 ns for 18-MHz sampling.

6 Mechanical characteristics

6.1 General

This clause defines the mechanical specifications for the interface of digital video systems used in environments where the physical distance between devices is limited and the general physical environment can be termed interior.

6.2 Interconnecting cable characteristics

The interface is designed to operate with a nominal signal pair impedance of 110 ohms.

6.2.1 Cable length

The majority of applications of this interface involve lengths less than 50 m for 13.5-MHz sampling and 40 m for 18-MHz sampling. For these lengths, cables with reasonable uniformity will generally give satisfactory results. For cable lengths greater than 50 m for 13.5-MHz sampling and 40 m for 18-MHz sampling, the cable and termination characteristics become more critical, in some cases requiring equalization.

6.2.2 Cable construction

The cable shall contain 12 pairs of conductors of which 11 pairs shall be used as signal lines. The remaining pair shall be used as system ground.

The cable shall be constructed to minimize the effects of crosstalk between signal lines, the susceptibility of the signal lines to external noise, and the transmission of interface signals to the external environment.

The cable shall contain an overall shield to minimize radiation, carried through the cable assembly and connectors via the cable shield pins and the connector body at each end.

The cable shall be constructed to minimize the differential delay between any two conductor pairs.

6.3 Connector characteristics

6.3.1 Mechanical considerations

The connectors shall have the mechanical characteristics conforming to the industry standard 25 contact D subminiature connector described below. Additional information may be found in MIL-C-24308C.

(Most applications of this interface require that the connectors be inserted many times. ECL voltage and current levels are relatively low. The materials used in the connector should be appropriate to the application.)

6.3.2 Connector contact assignments

The connector contact assignments shall be in accord with table 5.

6.3.3 Cable connector assembly

Cable connectors employ pin contacts and equipment connectors employ socket contacts (see figure 6).

6.3.4 Connector retaining mechanism

The cable connectors shall be provided with #4-40 mounting screws and the equipment connectors shall be provided with female screw locks or mating threads as shown in annex B.

Table 5 – Connector contact assignments

Pin	Signal line	Pin	Signal line
1	Clock	14	Clock return
2	System ground A	15	System ground B
3	DATA 9	16	DATA 9 return
4	DATA 8	17	DATA 8 return
5	DATA 7	18	DATA 7 return
6	DATA 6	19	DATA 6 return
7	DATA 5	20	DATA 5 return
8	DATA 4	21	DATA 4 return
9	DATA 3	22	DATA 3 return
10	DATA 2	23	DATA 2 return
11	DATA 1	24	DATA 1 return
12	DATA 0	25	DATA 0 return
13	Cable shield		

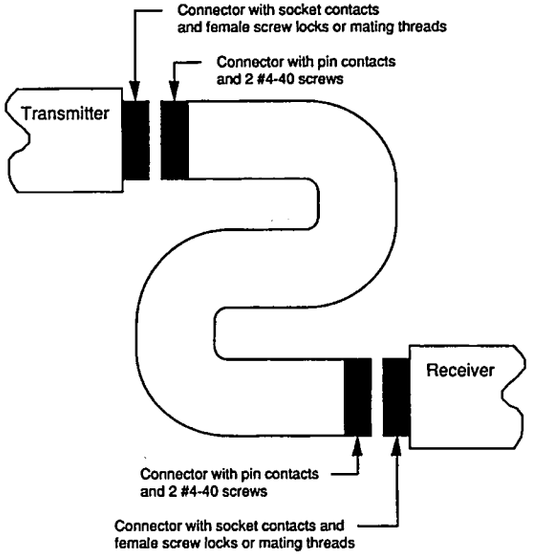


Figure 6 – Cable connector assembly

Annex A (normative)
ECL 10,000 and 10H000 parameters

A.1 Standard ECL parameters

"Standard ECL" in this application means an integrated circuit device of the ECL 10,000 or 10H000 series or equivalent. Typical key parameters are:

System power supply (V): –4.7 V to -5.7 V; –5.2 V nominal;

Logic states with respect to ground (typical): "1" = –0.8 V = High (H); "0" = –1.85 V = Low (L);

Output impedance: Open emitter-follower output (7 ohm typical) to drive terminated lines;

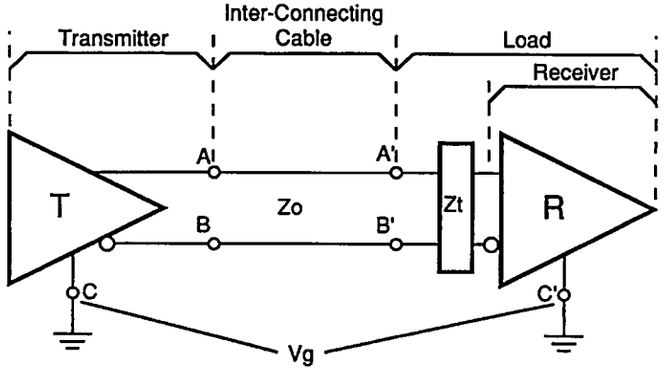
Propagation delay ECL 10,000: 2-3 ns per gate; typical edge speeds are 2-3 ns (20% to 80%);

Propagation delay ECL 10H000: 1-2 ns per gate; typical edge speeds are 1-2 ns (20% to 80%).

A.2 Balanced interface circuit

Each circuit consists of three parts as shown in figure A.1: the line driver, the balanced interconnecting cable, and the load. The line driver is comprised of a single transmitter (T) with a low-output impedance. The load is comprised of a single receiver (R), and a cable termination impedance (Zt).

Electrical characteristics of the receiver without cable termination shall conform to standard balanced ECL specifications. Use of a cable termination (Zt) is mandatory. Zt shall be nominally 110 ohms.



A, A' = data line
B, B' = return line
Zt = cable termination
A, B = transmitter interface points
A', B' = load interface points
C = transmitter circuit ground
C' = load circuit ground
Vg = ground potential difference
Zo = cable characteristic impedance

Figure A.1 – Balanced interface circuit

Annex B (normative)
Connector characteristics

The interface employs the 25 contact D subminiature connector, with the connectors on the transmitter and receivers using socket contacts and the connectors on the cable both using pin contacts. Connectors are locked together by two #4-40 screws on the cable connectors, which go in female screw locks mounted on the equipment connector.

Detailed dimensions for the connector are given in MIL-C-24308C.

The relative position of the connector and the female screw lock is defined in figure B.1. Recommended minimum connector spacing is defined in figure B.2.

It is recommended that the cable connectors employ a conductive backshell to maintain shielding of the signal conductors. Care must be taken to select designs that are appropriate for use with the screw-latching method specified.

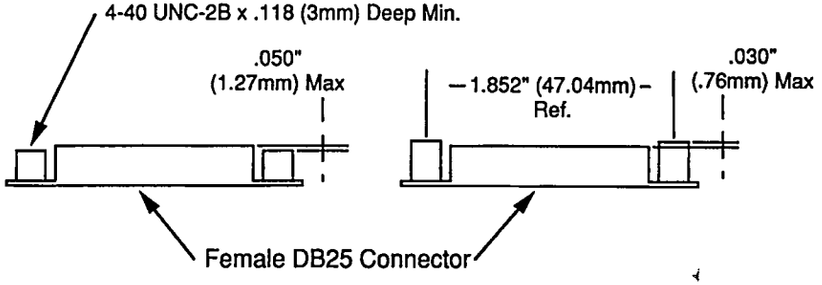


Figure B.1 – Female screw lock mounting

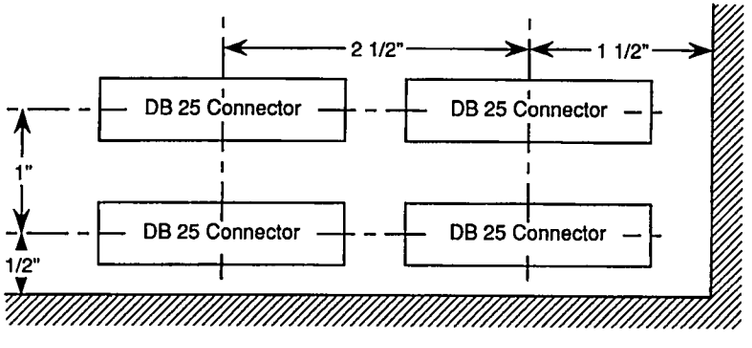


Figure B.2 – Minimum connector spacing

Annex C (informative)
Cable shield pin

The cable shield (pin 13) is for the purpose of controlling electromagnetic radiation from the cable. It is recommended that pin 13 provide high-frequency continuity to the chassis ground at both ends and, in addition, provide DC continuity to the chassis ground at the transmit end.

Annex D (informative)
Connector orientation

Vertical or horizontal mounting: Contact 1 uppermost.

Annex E (informative)
Monochrome operation

Monochrome operation at 29.97 Hz frame rate can be achieved by setting the color-difference signals (C_B, C_R) to zero (200_H).

Annex F (informative)
Error detection and correction in the video timing reference signal

Table F.1 enables single-bit errors in the fourth bytes of EAV and SAV to be corrected. Double errors, and some multiple-bit errors, are detected but not corrected. The table gives corrected values for bits 8, 7, and 6 where possible. Multiple errors are denoted by asterisks.

Table F.1 – Error correction table

Received P3 – P0	Received bits 8, 7, and 6 (F, V, and H)							
	000	001	010	011	100	101	110	111
0000	000	000	000	*	000	*	*	111
0001	000	*	*	111	*	111	111	111
0010	000	*	*	011	*	101	*	*
0011	*	*	010	*	100	*	*	111
0100	000	*	*	011	*	*	110	*
0101	*	001	*	*	100	*	*	111
0110	*	011	011	011	100	*	*	011
0111	100	*	*	011	100	100	100	*
1000	000	*	*	*	*	101	110	*
1001	*	001	010	*	*	*	*	111
1010	*	101	010	*	101	101	*	101
1011	010	*	010	010	*	101	010	*
1100	*	001	110	*	110	*	110	110
1101	001	001	*	001	*	001	010	*
1110	*	*	*	011	*	101	110	*
1111	*	001	010	*	100	*	*	*

Annex G (informative)
Picture centering

Relative horizontal picture centering for 13.5-MHz and 18-MHz sampling structures is shown in figure G.1.

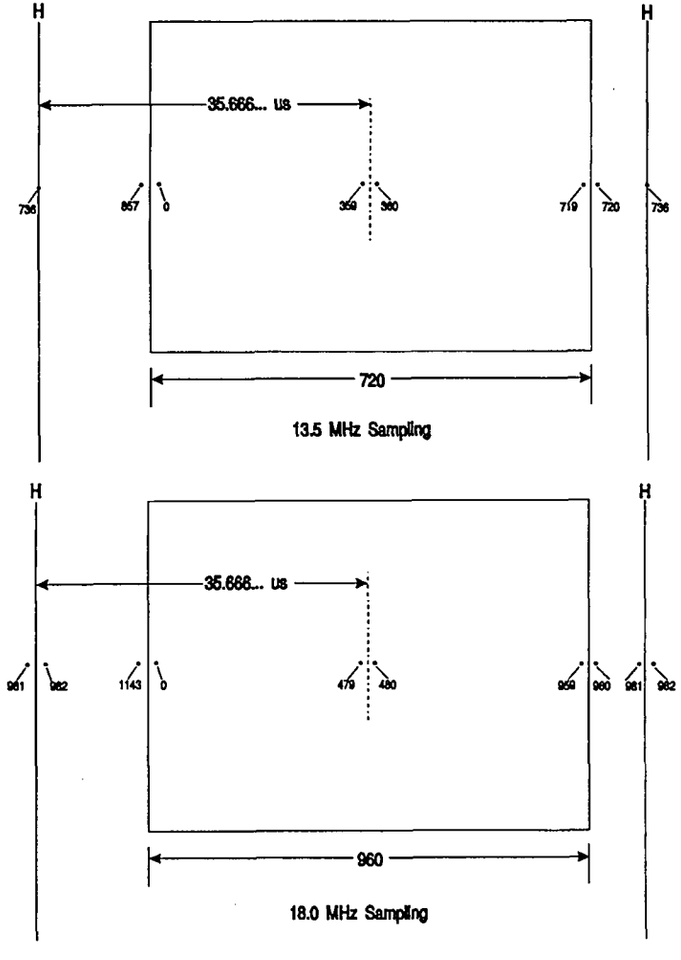


Figure G.1 – Horizontal picture centering for 525/59.94 component systems

Annex H (informative)
Bibliography

ANSI/SMPTE 125M-1992, Television — Component Video Signal 4:2:2 — Bit-Parallel Digital Interface

ANSI/SMPTE 259M-1993, Television — 10-Bit 4:2:2 Component and $4f_{sc}$ NTSC Composite Digital Signals — Serial Digital Interface

MIL-C-24308C, General Specification for Connectors, Electric, Rectangular, Nonenvironmental, Miniature, Polarized Shell, Rack and Panel

ITU-R 601-2, Encoding Parameters of Digital Television for Studios

ITU Report 962-1, The Filtering, Sampling and Multiplexing for Digital Encoding of Colour Television Signals

Documents are in preparation to cover auxiliary signals (HANC, VANC, DVITC, and video index), but are not yet available.

PROPOSED SMPTE STANDARD

SMPTE 274M

for Television —

1920 × 1080 Scanning and Interface

Contents

1 Scope

1.1 This standard defines a family of raster-scanning systems for the representation of stationary or moving two-dimensional images sampled temporally at a constant frame rate and having an image format of 1920 × 1080 and an aspect ratio of 16:9 as given in table 1. This standard specifies:

- R′G′B′ color encoding;
- R′G′B′ analog and digital interfaces;
- $Y'P'_BP'_R$ color encoding and analog interface;
- $Y'C'_BC'_R$ color encoding and digital interface.

An auxiliary component A may optionally accompany $Y'C'_BC'_R$; this interface is denoted $Y'C'_BC'_RA$.

Work is in progress to define further versions of the 1920 × 1080 format at a number of frame rates, including 24/1.001, 24, 25, 30/1.001, 30, and 50 frames per second.

Table 1 – Scanning systems

	System nomenclature	Samples per active line (S/AL)	Lines per picture height (L/PH)	Frame rate (Hz)	Scanning format	Sampling frequency f_s (MHz)	Samples per total line (S/TL)	Total lines per frame
1	1920 × 1080/60/1:1	1920	1080	60	Progressive	148.5	2200	1125
2	1920 × 1080/59.94/1:1	1920	1080	$\frac{60}{1.001}$	Progressive	$\frac{148.5}{1.001}$	2200	1125
3	1920 × 1080/60/2:1	1920	1080	30	2:1 Interlace	74.25	2200	1125
4	1920 × 1080/59.94/2:1	1920	1080	$\frac{30}{1.001}$	2:1 Interlace	$\frac{74.25}{1.001}$	2200	1125

2 Normative references

The following standards contain provisions which, through reference in this text, constitute provisions of this standard. At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the standards listed below.

SMPTE 240M-1994, Television — Signal Parameters — 1125-Line High-Definition Production Systems

SMPTE RP 177-1993, Derivation of Basic Television Color Equations

CIE Publication 15.2 (1986), Colorimetry, Second Edition

IEC 169-8 (1978), R.F. Coaxial Connectors with Inner Diameter of Outer Conductor 6.5 mm (0.256 in) with Bayonet Lock — Characteristic Impedance 50 Ohms (Type BNC).

ITU-R BT.709, Basic Parameter Values for the HDTV Standard for the Studio and for International Programme Exchange

3 General

3.1 The specification of a system claiming compliance with this standard shall state:

- which of the scanning systems of table 1 are implemented;

- which of the analog R′G′B′ or $Y'P'_BP'_R$ and/or which of the digital R′G′B′, $Y'C'_BC'_R$, or $Y'C'_BC'_RA$ interfaces are implemented;

- whether the system implements the system colorimetry or interim implementation; and

- whether the digital representation employs eight bits or ten bits.

3.2 Digital code word values in this standard are expressed as decimal values in the ten-bit representation. An eight-bit system shall round or truncate to the most significant eight bits according to provisions to be described.

4 Scanning

4.1 Scanning shall be based on a reference clock of the sampling frequency indicated in table 1, which shall be maintained to a tolerance of ± 10 ppm.

4.2 A frame shall comprise the indicated total lines per frame, each of equal duration determined by the sampling frequency and the samples per total line (S/TL). Each line shall be uniformly scanned from left to right; lines in a frame shall be uniformly scanned from top to bottom. Lines are numbered in time sequence according to the raster structure described in clause 7.

4.3 Timing instants in each line shall be defined with respect to a horizontal datum denoted by 0_H which is established by horizontal synchronizing (sync) information in clauses 9 and 15. Each line shall be divided into a number of reference clock intervals, of equal duration, indicated by the column S/TL in table 1.

4.4 A progressive system shall convey 1080 active picture lines per frame in order top to bottom.

4.5 An interlaced system shall scan a frame as a first field then a second field, in which the scan lines of each field have twice the vertical spatial sampling pitch of the frame. Scanning lines in the second field shall be displaced vertically by the vertical sampling pitch, and scanning timing shall be delayed temporally by half the frame time, from scanning lines in the first field.

The first field shall convey 540 active picture lines, starting with the top picture line of the frame. The second field shall convey 540 active picture lines, ending with the bottom picture line of the frame.

5 System colorimetry

5.1 New equipment should be designed in accordance with the colorimetric analysis and optoelectronic transfer function defined in this clause. This corresponds to ITU-R BT.709.

5.2 Digital representation and treatment of wide-gamut color signals, are not specified in the

7.9 The center of the picture shall be located at the center of the clean aperture (and of the production aperture), midway between samples 1151 and 1152, and midway between lines 581 and 582 in a progressive system, and midway between lines 291 and 853 in an interlaced system.

7.10 Each edge of the picture width, measured at the 50% amplitude point, shall lie within six reference clock intervals of the production aperture.

8 Digital representation

8.1 Digital representation shall employ either R′G′B′ or Y′C′$_B$C′$_R$ components as defined in clauses 5 or 6, uniformly sampled.

8.2 The digital signals described here are assumed to have been filtered to reduce or prevent aliasing upon sampling (see annex B).

8.3 R′G′B′ signals and Y′ signals shall have bandwidth nominally 60 MHz for progressive systems and 30 MHz for interlaced systems. C′$_B$C′$_R$ signals shall have bandwidth nominally half that of the associated Y′ signal.

8.4 R′G′B′ signals and the Y′ signal of the Y′C′$_B$C′$_R$ interface shall be sampled orthogonally, line- and picture-repetitive, at the sampling frequency, f_s. The period of the sampling clock shall be denoted T.

8.5 A sampling instant in a line is denoted in this standard by a number from 0 through one less than the total number of samples in a line. Sample number zero corresponds to the 0_H datum. The sample numbering is shown in figure 3.

8.6 Sampled data at the interface shall be such that appropriate $\sin(x)/x$ correction occurs during conversion of the signal to the analog domain.

8.7 Digital R′, G′, B′, and Y′ components shall be computed as follows:

$$L'_d = \lfloor 219DL' + 16D + 0.5 \rfloor; \quad D = 2^{n-8}$$

where L′ is the component value in abstract terms from zero to unity, n takes the value 8 or 10 corresponding to the number of bits to be represented and L'_d is the resulting digital code. The operator $\lfloor x \rfloor$ denotes floor, the largest integer not greater than its argument.

NOTE – This scaling places the extrema of R′, G′, B′, and Y′ components at code words 64 and 940 in a ten-bit representation or code words 16 and 235 in an eight-bit representation.

8.8 Digital C′$_B$ and C′$_R$ components of the Y′C′$_B$C′$_R$ set shall be computed as follows:

$$C'_d = \lfloor 224DC' + 128D + 0.5 \rfloor; \quad D = 2^{n-8}$$

where C′ is the component value in abstract terms from – 0.5 to + 0.5 and C'_d is the resulting digital code.

NOTE - This scaling places the extrema of C′$_B$ and C′$_R$ at code words 64 and 960 in a ten-bit representation or code words 16 and 240 in an eight-bit representation.

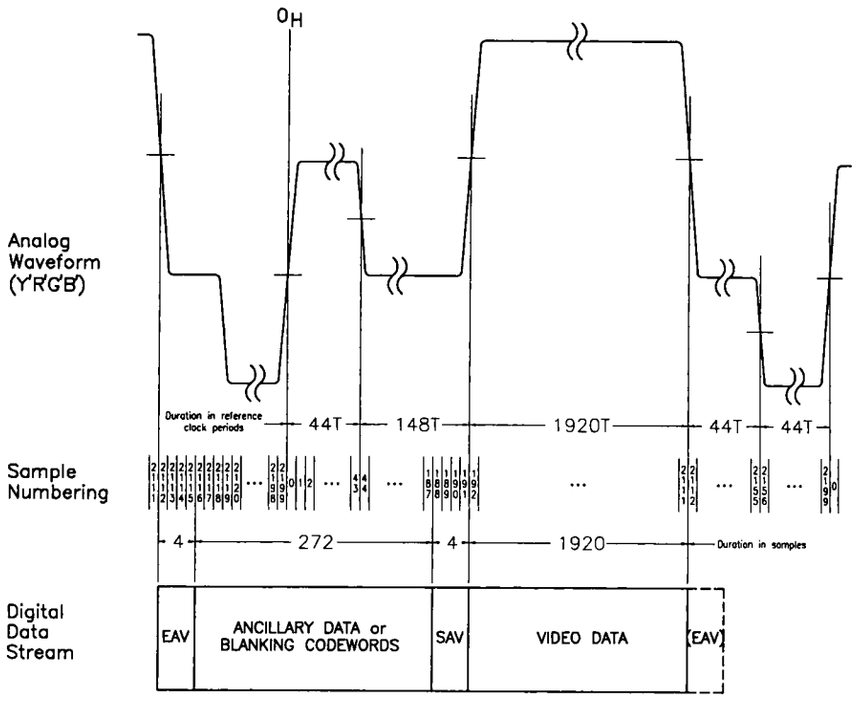
8.9 C′$_B$ and C′$_R$ signals shall be horizontally subsampled by a factor of two with respect to the Y′ component. C′$_B$ and C′$_R$ samples shall be cosited with even-numbered Y′ samples (see annex B).

8.10 Code values having the eight most-significant bits all zero or all one — that is, ten-bit codes 0, 1, 2, 3, 1020, 1021, 1022 and 1023 — are employed for synchronizing purposes and shall be prohibited from video or ancillary data.

8.11 A system having an eight-bit interface may round video signals to eight bits and then discard the two least-significant bits. The two least-significant bits of all other data across the interface shall be truncated without rounding.

8.12 For Y′, R′, G′, and B′ signals, undershoot and overshoot in video processing may be accommodated by the use of code words 4 through 63 and code words 941 through 1019 in a ten-bit system, or code words 1 through 15 and code words 236 through 254 in an eight-bit system.

For C′$_B$ and C′$_R$ signals, undershoot and overshoot in video processing may be accomodated by the use of code words 4 through 63 and code words 961 through 1019 in a ten-bit system, or code words 1 through 15 and code words 241 through 254 in an eight-bit system.



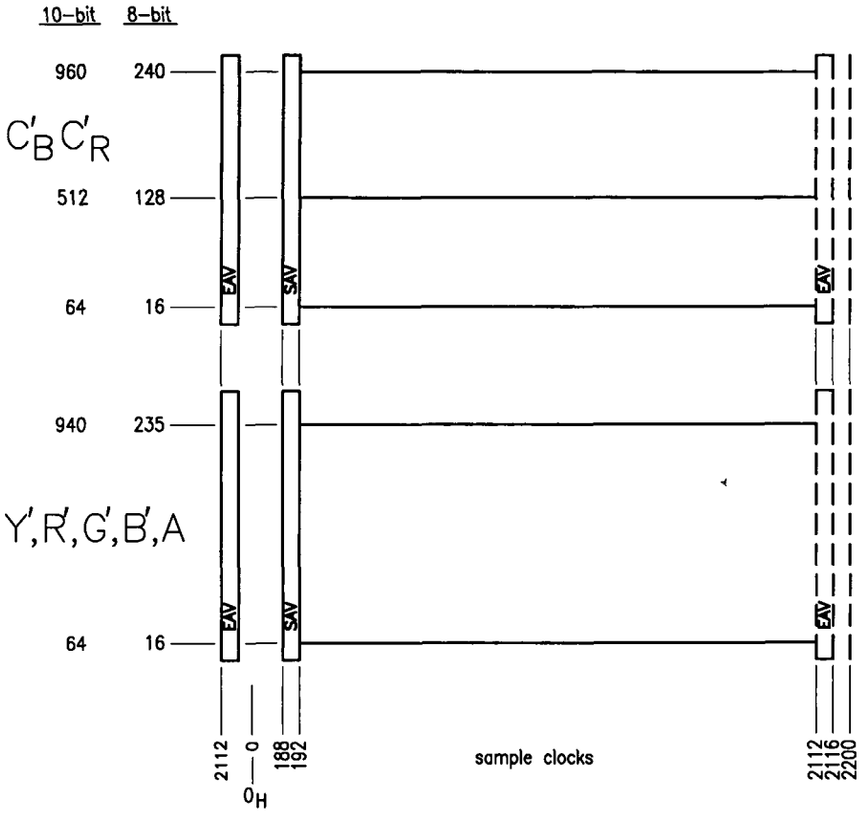
NOTES
1 Horizontal axis not to scale.
2 The sampling instant occurs at the leading edge of each numbered sample.
3 A line of digital video extends from the first word of EAV through the last word of video data.

Figure 3 — Analog and digital timing relationships

9 Digital timing reference sequences (SAV, EAV)

9.1 SAV (start of active video) and EAV (end of active video) digital synchronizing sequences shall define synchronization across the digital interface. Figures 2 and 4 show the relationship of the SAV and EAV sequences to analog video and digital video.

9.2 An SAV or EAV sequence shall comprise four consecutive code words: a code word of all ones, a code word of all zeros, another code word of all zeros, and a code word including F (field/frame), V, H (horizontal), P3, P2, P1, and P0 (parity) bits. An SAV sequence shall be identified by having H= 0; EAV shall have H= 1 (tables 2 and 3 show details of the coding).



NOTE — See also figure 3.

Figure 4 – Digital interface, horizontal timing details

Table 2 – Video timing reference codes

Bit number		9 (MSB)	8	7	6	5	4	3	2	1	0 (LSB)
Word	Value										
0	1023	1	1	1	1	1	1	1	1	1	1
1	0	0	0	0	0	0	0	0	0	0	0
2	0	0	0	0	0	0	0	0	0	0	0
3		1	F	V	H	P3	P2	P1	P0	0	0

Table 3 – Protection bits for SAV and EAV

Bit number	9	8	7	6	5	4	3	2	1	0
Function	1 Fixed	F	V	H	P3	P2	P1	P0	0 Fixed	0 Fixed
0	1	0	0	0	0	0	0	0	0	0
1	1	0	0	1	1	1	0	1	0	0
2	1	0	1	0	1	0	1	1	0	0
3	1	0	1	1	0	1	1	0	0	0
4	1	1	0	0	0	1	1	1	0	0
5	1	1	0	1	1	0	1	0	0	0
6	1	1	1	0	1	1	0	0	0	0
7	1	1	1	1	0	0	0	1	0	0

9.3 Every scan line shall include a four-sample EAV sequence commencing 88 clocks prior to 0_H, and a four-sample SAV sequence commencing 188 clocks after 0_H. The EAV sequence immediately preceding the 0_H datum of line 1 shall be considered to be the start of the digital frame.

9.4 In a progressive system:

– The EAV and SAV of all lines shall have F=0.

NOTE – In future progressive scan systems, if there are two different types of frames (such as number of lines), the differentiation between frames shall be indicated by the F-bit.

– The EAV and the SAV of lines 1 through 41 inclusive and lines 1122 through 1125 inclusive, shall have V=1;

– The EAV and SAV of lines 42 through 1121 inclusive, shall have V= 0.

9.5 In an interlaced system:

– The EAV sequence of line 1 shall be considered to be the start of the first digital field and the EAV sequence of line 563 shall be considered to be the start of the second digital field;

– The EAV and SAV of lines 1 through 562 inclusive shall have F= 0. The EAV and SAV of lines 563 through 1125 inclusive shall have F= 1;

– The EAV and SAV of lines 1 through 20, lines 561 through 583, and lines 1124 and 1125 shall have V= 1;

– The EAV and the SAV of lines 21 through 560 and lines 584 through 1123 shall have V= 0.

9.6 A line, which in the analog representation is permitted to convey ancillary signals, may convey digitized ancillary signals.

NOTE – The inclusion of line-number information, following the EAV sequence, is under study.

10 Ancillary data

10.1 Ancillary data may optionally be included in the blanking intervals of a digital interface according to this standard.

10.2 Any interval between EAV and SAV may be employed to convey ancillary data packets.

10.3 The interval between SAV and EAV of any line that is outside the vertical extent of the picture, and that is not employed to convey digitized ancillary signals, may be employed to convey ancillary data packets.

10.4 Independent ancillary data packets may be conveyed across each of the three R′, G′, and B′ channels, or across each of the three Y′, C'_B/C'_R, and A channels.

10.5 In the case of 10-bit representation, intervals not used to convey SAV, video data, EAV, or ancillary data shall convey the code word 64 (black) in the R′, G′, B′, Y′, or A channels, or 512 in the C'_B/C'_R channels. They shall be 16 and 128 respectively in the case of 8-bit representation.

10.6 In the case of 10-bit representation, code words 1, 2, 3, 1020, 1021, 1022, and 1023 shall be prohibited from ancillary data words. In the case of 8-bit representation, code words 1 and 255 shall be prohibited from ancillary data words.

NOTE – Specifications of the details of ancillary data will be the subject of future SMPTE standards.

11 Bit-parallel electrical interface

11.1 This clause describes a bit-parallel point-to-point electrical interface with one transmitter and one receiver. The interface may be used to convey R′G′B′ components, $Y'C'_BC'_R$ components, or $Y'C'_BC'_R$ components augmented by an auxiliary component A coded similarly to video but otherwise outside the scope of this standard.

11.2 Video data shall be transmitted in NRZ form in real time (unbuffered) in blocks, each comprising one active line.

11.3 A pair of conductors conveys a clock signal at the sampling rate of Y′ (or R′G′B′).

11.4 Data shall be transmitted in parallel by means of eight or ten shielded conductor pairs for each of the channels.

11.5 The signals on the interface shall be transmitted without equalization in the interlaced system for a distance of up to 20 m (65.6 ft), and in the progressive system for a distance of up to 14 m (46.3 ft).

11.6 The data bits of each component shall be numbered nine through zero, where zero is the least significant bit.

11.7 The R′G′B′ interface shall use three sets of the same number of either eight or ten pairs to convey R′, G′, and B′ components on the contacts shown in table 4.

11.8 The $Y'C'_BC'_R$ interface uses a set of eight or ten pairs to convey the Y′ signal (on the pins indicated for the G′ signals in table 4), and a second set of the same number of pairs to convey time-multiplexed C'_B and C'_R signals (on the pins indicated for R′ in table 4). C'_B and C'_R signals shall be time-multiplexed by sample basis in the order of C'_B and C'_R.

11.9 The $Y'C'_BC'_RA$ interface conveys eight or ten bits of $Y'C'_BC'_R$ as above, and conveys an auxiliary signal A of the same number of bits (on the pins indicated for B′ in table 4).

12 Electrical characteristics

12.1 The arrangement of the transmitter and receiver devices and conductors for one balanced conductor pair shall be as shown in figure 5.

NOTE – The transmitter and receiver parameters are ECL-compatible so as to permit, in the interlaced system, the use of standard ECL (10KH series) devices.

Table 4 – 93-contact connector contact assignments

	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
	1	CK+	17	GND	33	CK–						
MSB	2	G9+	18	GND	34	G9–	49	B4+	64	GND	79	B4–
	3	G8+	19	GND	35	G8–	50	B3+	65	GND	80	B3–
	4	G7+	20	GND	36	G7–	51	B2+	66	GND	81	B2–
	5	G6+	21	GND	37	G6–	52	B1+	67	GND	82	B1–
	6	G5+	22	GND	38	G5–	53	B0+	68	GND	83	B0–
	7	G4+	23	GND	39	G4–	54	R9+	69	GND	84	R9–
	8	G3+	24	GND	40	G3–	55	R8+	70	GND	85	R8–
LSB_8	9	G2+	25	GND	41	G2–	56	R7+	71	GND	86	R7–
	10	G1+	26	GND	42	G1–	57	R6+	72	GND	87	R6–
LSB_{10}	11	G0+	27	GND	43	G0–	58	R5+	73	GND	88	R5–
	12	B9+	28	GND	44	B9–	59	R4+	74	GND	89	R4–
	13	B8+	29	GND	45	B8–	60	R3+	75	GND	90	R3–
	14	B7+	30	GND	46	B7–	61	R2+	76	GND	91	R2–
	15	B6+	31	GND	47	B6–	62	R1+	77	GND	92	R1–
	16	B5+	32	GND	48	B5–	63	R0+	78	GND	93	R0–

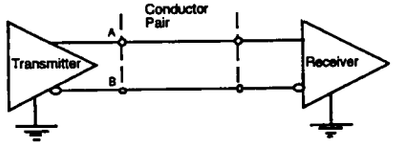


Figure 5 – Transmitter and receiver connection

12.2 The signalling polarity of voltage appearing across the interface shall be positive binary, defined as follows:

– The A terminal of the line driver shall be negative with respect to the B terminal for a binary 0 state.

– The A terminal of the line driver shall be positive with respect to the B terminal for a binary 1 state.

12.3 The transmitter in an eight-bit system shall assert bits 1 and 0 to logic zero.

12.4 The receiver in an eight-bit system shall terminate bit pairs 1 and 0.

12.5 The transmitter shall have a balanced output with a maximum impedance of 110 Ω.

12.6 The average of the voltages on the two terminals of the line driver with reference to the ground terminal shall be –1.29 V ± 15%.

12.7 The generated signal shall lie between 0.6 V peak-to-peak and 2.0 V peak-to-peak, measured across a 110-Ω resistor connected to the output terminals without any transmission line.

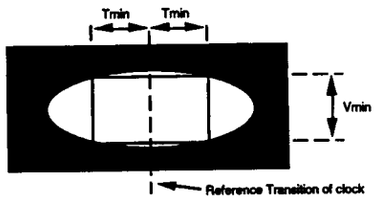
12.8 Rise and fall times shall be no greater than 0.15T when measured between the 20% and the 80% amplitude points across a 110-Ω resistive load. The difference between rise and fall times shall not exceed 0.075T.

12.9 The receiver shall present an impedance of 110 Ω ± 10 Ω.

12.10 Maximum input signal amplitude shall be 2.0 V peak-to-peak.

12.11 The receiver shall require a differential input voltage of no more than 185 mV peak to peak to correctly attain the intended binary state. Additionally, the line receiver must sense correctly the binary data when a random data

signal produces, at the data detection point, the conditions represented by the eye diagram shown in figure 6.



Tmin = 0.3T
Vmin = 100 mV

NOTE — Cable response losses, frequency response characteristics of the interface electronics, propagation delay skew, data source timing skew, and clock jitter all affect reliable detection of received data, and must be taken into account in system timing margin considerations. This figure assumes propagation skew of 0.18T, data source skew of 0.075T, and clock jitter of 0.04T to show the minimum eye opening of 2 x Tmin, due only to frequency characteristics of the cable and interface electronics. In this case, the total system timing margin goes to zero.

Figure 6 – Idealized eye diagram corresponding to the minimum input signal level

12.12 The receiver shall operate correctly in the presence of common mode noise (comprising interference in the range 0 to line frequency, f_H, with both terminals to ground) having a maximum amplitude of 0.3 V.

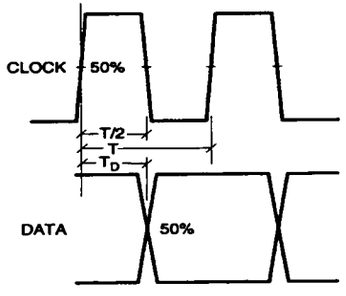
12.13 Data shall be correctly sensed when the relative differential delay between the received clock and the received data is less than 0.3T.

13 Clock

13.1 One pair on the interface shall convey a clock signal at the sampling frequency, which shall have a positive pulse width of (0.5 ± 0.11) T.

13.2 Peak-to-peak jitter between rising edges of the transmitted clock shall be less than 0.08T, measured over a period of one frame.

13.3 Data signals shall be asserted by the transmitter at a time interval (0.5 ± 0.075)T, denoted T_D, following 0-to-1 transition of the clock, according to figure 7.



Clock period, T = $1/(2200f_H)$
Clock pulse width, t = (0.5± 0.11)T
Data timing (sending end), T_D = (0.5± 0.075)T

Figure 7 — Clock-to-data timing (at sending end)

13.4 Data signals shall be sampled at the receiver by the 0-to-1 transition of the clock.

14 Bit-parallel mechanical interface

14.1 The multichannel cable shall consist of twisted-pair conductors with individual shields. The nominal characteristic impedance of each twisted pair shall be 110 Ω.

14.2 This standard applies to applications where the physical length of the cable is at most 20 m for interlaced systems and 14 m for progressive systems. Within this range, equalization of the cable characteristics is not required.

14.3 The multichannel cable shall consist of either 21 or 31 twisted-pairs of conductors with individual shielding of each pair. The cable should be constructed to minimize the

differential delay between any two conductor pairs. Cable with controlled differential delay may be appropriate for transmission distances longer than that specified in 14.2.

14.4 The cable shall contain an overall shield to minimize electromagnetic interference (EMI) carried through the cable assembly and connectors via the cable shield and the connector bodies.

14.5 An interface according to this standard shall employ a 93-pin connector. Figures 8, 9, and 10 show the mechanical drawings and dimensions of the pin connector (cable plug), the socket connector (equipment receptacle), and the connector metal hood and retaining mechanism, respectively. The cable assembly shall provide pin contacts at both ends. Transmitter and receiver equipment shall have connectors with socket contacts. The connector hood shall be designed to prevent radiation of electromagnetic interference.

14.6 Connector contact assignment shall be according to table 4. The shield for each conductor pair shall use the ground pin located between pins for the signal pair as shown in table 4.

14.7 The overall shield of the multichannel cable shall be electrically connected to the connector hood. The connector hood, in turn, shall be grounded to the frame of the equipment. The shield wire of each twisted pair shall be grounded to the system ground of the equipment through a pin contact. There shall be electrical conduction between the overall cable shield and the connector hood and equipment frame.

14.8 The cable connectors shall be provided with two M4 mounting screws and the equipment connectors shall be provided with two M4 female screws.

15 Analog sync

15.1 Details of analog sync timing are shown in figures 1, 3, and 11, and are summarized in table 5. The parameter F not shown in these figures is the duration of the rising edge of horizontal sync pulse.

Table 5 – Analog sync timing

		Duration (T)	Tolerance (T)
a	See figure 11	44	± 3
b	See figure 11	2112	−6 +0
c	See figure 11	44	± 3
d	See figure 11	132	± 3
e	See figure 11	192	−0 +6
f	Sync rise time	4	± 1.5
g	See figure 11	1100	
h	See figure 11	1012	± 3
	Total line	2200	
	Active line	1920	−12 +0

15.2 A positive zero-crossing of a trilevel sync pulse shall define the 0_H datum for each line. A negative-going transition precedes this instant by 44 reference clock intervals, and another negative-going transition follows this instant by 44 reference clock intervals.

15.3 Positive transition of a trilevel sync pulse shall be skew symmetric with a rise time from 10% to 90% of 4 ± 1.5 reference clock periods. The midpoint of each negative transition shall be coincident with its ideal time within a tolerance of ± 3 reference clock periods.

15.4 The trilevel sync pulse shall have structure and timing according to clause 7. The positive peak of sync shall have a level of +300 mV± 6 mV; its negative peak shall have a level of –300 mV ± 6 mV. The amplitude difference between positive and negative sync pulses shall be less than 6 mV.

15.5 Each line that includes a vertical sync pulse shall maintain blanking level, here denoted zero, except for the interval(s) occupied by sync pulses. During the horizontal blanking interval, areas not occupied by sync shall be maintained at blanking level, here denoted zero.

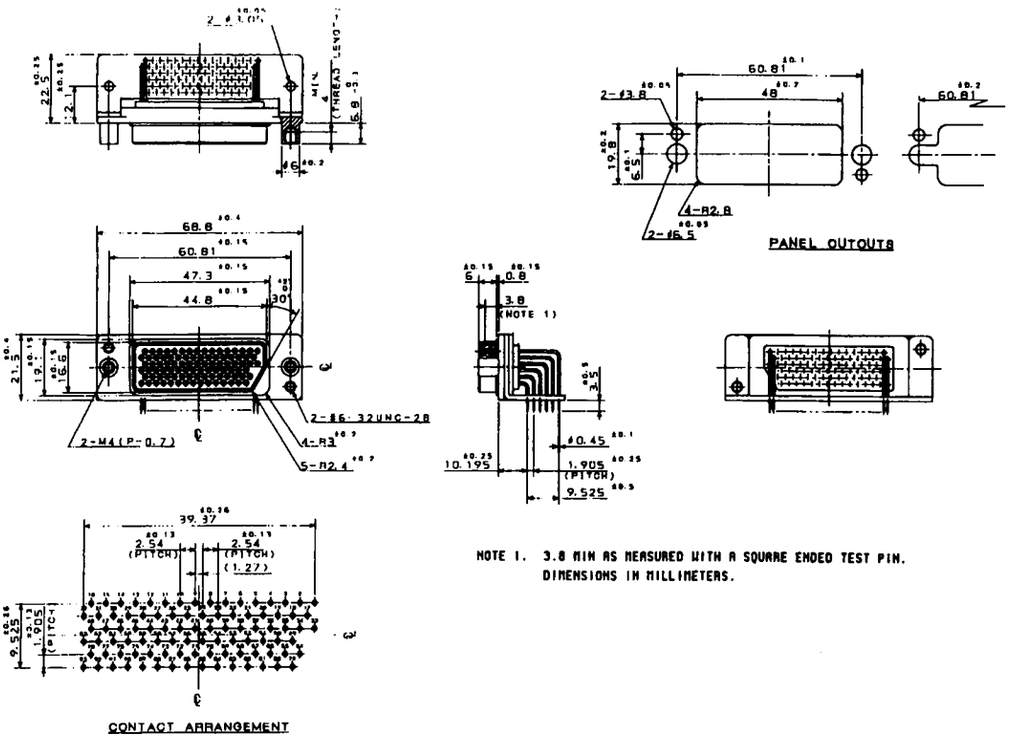


Figure 9 – 93-contact socket connector (equipment)

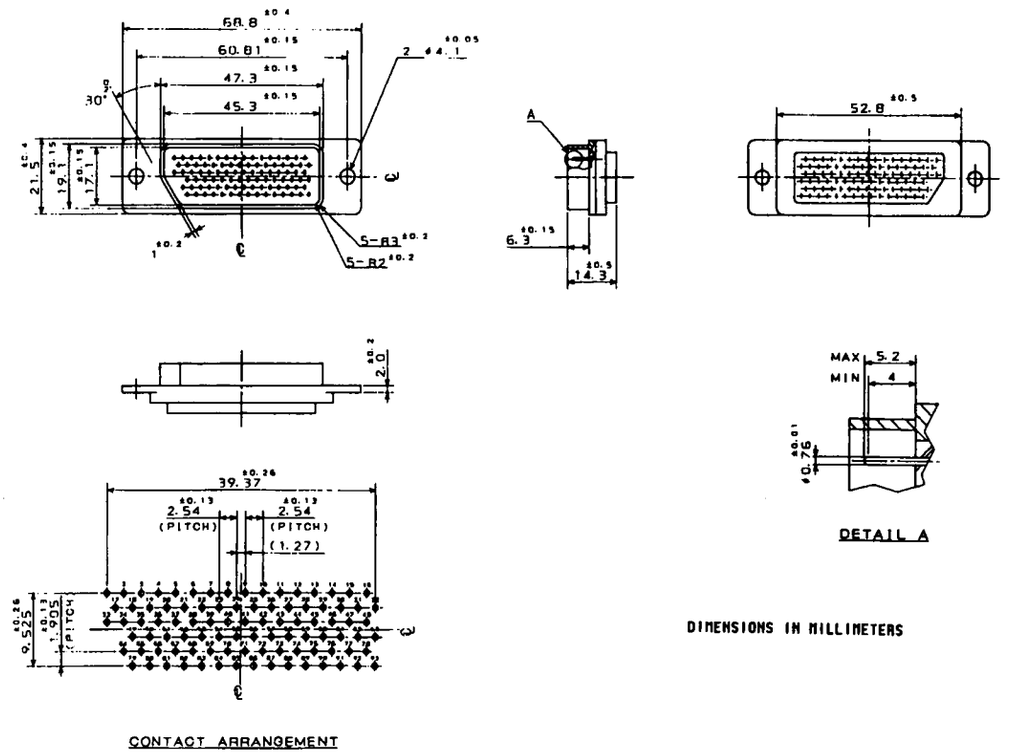


Figure 8 – 93-contact plug connector (cable)

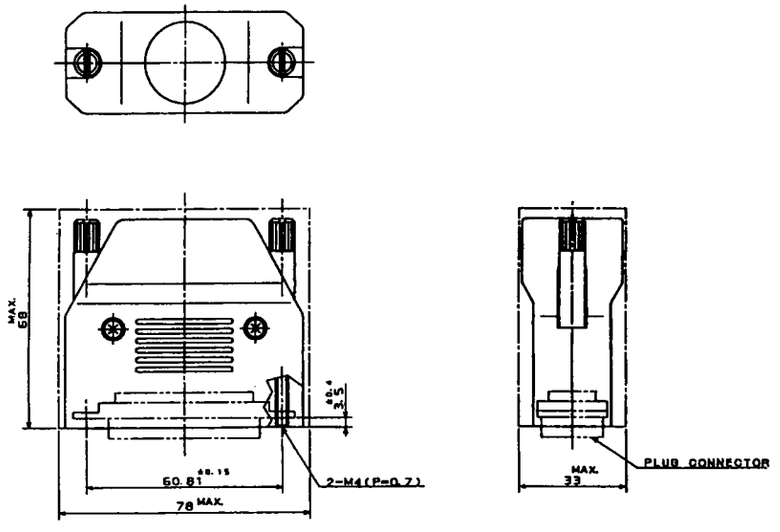


Figure 10 – 93-contact plug (hood)

15.6 In addition to the trilevel sync pulse that defines 0_H, a vertical sync line shall include a midline trilevel sync pulse whose elements are delayed from 0_H by one-half the line duration.

Certain vertical sync lines may contain a broad pulse during the first half line, and may contain a broad pulse during the second half line, in the manner described in 15.7, 15.8, and 15.9. The leading 50% point of a broad pulse shall be 132T after the preceding trilevel zero-crossing; its duration shall be 880T (see figure 11).

15.7 In a progressive system, a frame shall commence with six vertical sync lines:

– five lines having broad pulses in both the first and second half lines; then

– one line having only a midpoint trilevel pulse.

15.8 The first field of an interlaced system shall commence with six vertical sync lines:

– five lines having broad pulses in both the first and second half lines; then

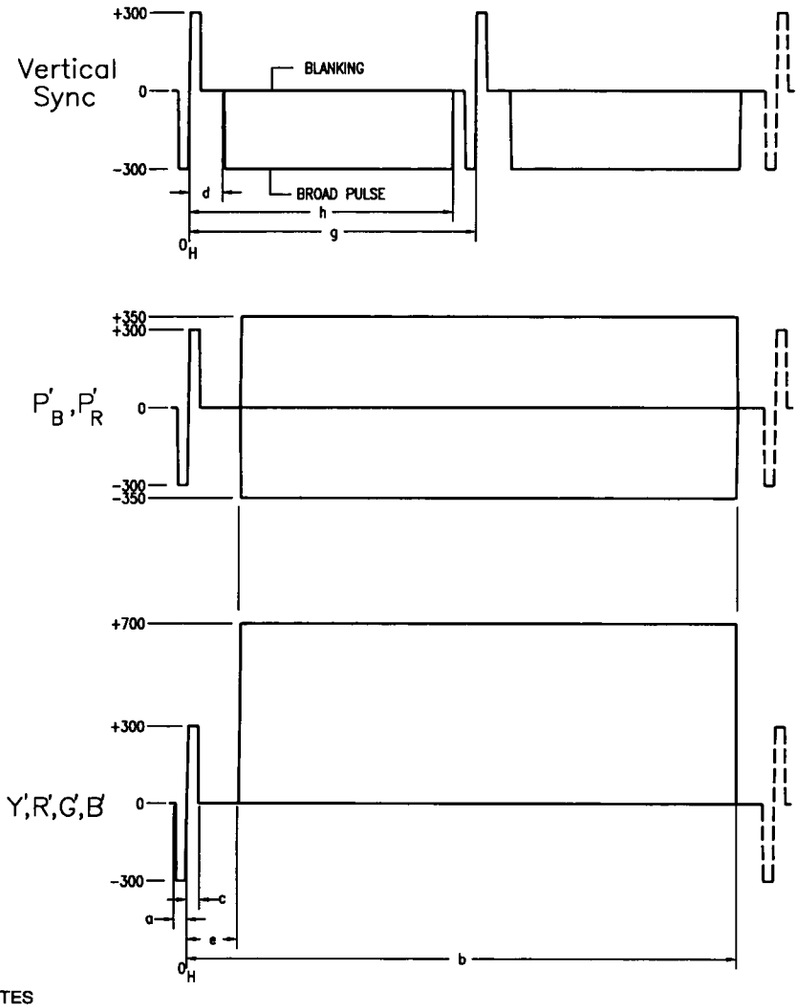
– one line having only a midpoint trilevel pulse.

15.9 The second field of an interlaced system shall commence with six vertical sync lines:

– a line having blanking in the first half line, a midline trilevel pulse, and a broad pulse in the second half line;

– four lines having broad pulses in both the first and second half lines; then

– one line having a broad pulse in the first half line.



NOTES
1 Values for a, b, c, d, e, g and h are given in table 5.
2 See also figure 3.

Figure 11 — Analog interface, horizontal timing details

16 Analog interface

16.1 An analog interface according to this standard may employ either the R'G'B' component set or the Y'P'$_B$P'$_R$ component set.

16.2 R'G'B' signals and Y' signals shall have bandwidth nominally 60 MHz for progressive systems and 30 MHz for interlaced systems.

16.3 P'$_B$P'$_R$ signals shall have 0.5 the bandwidth of the associated Y' signal.

16.4 Each component signal shall be conveyed electrically as a voltage on an unbalanced coaxial cable into a pure resistive impedance of 75 Ω.

16.5 For the Y' component, reference black (zero) in the expressions of clauses 5 and 6 shall correspond to a level of 0 Vdc, and reference white (unity) shall correspond to 700 mV.

16.6 P'$_B$ and P'$_R$ components are analog versions of the C'$_B$ and C'$_R$ components of 5.7 or 6.6, in which zero shall correspond to a level of 0 Vdc and reference peak level (value 0.5 of equations in 5.7) shall correspond to a level of +350 mV.

16.7 Trilevel sync according to clause 15 shall be added to each analog component.

16.8 Each of the electrical signals in an analog interface employs a connector that shall conform to IEC 169-8 with the exception that the impedance of the connector may be 75 Ω, or to SMPTE RP 160.

Annex A (informative)
Relationship to SMPTE 240M scanning

SMPTE 240M defines 1125/60 and 1125/59.94 interlaced systems having 1035 active picture lines. The first field has 517 active picture lines starting at line 41. The second field has 518 active picture lines starting with the top line of the picture at line 603 and including the bottom line of the frame at line 1120.

Annex B (informative)
Pre- and post-filtering characteristics

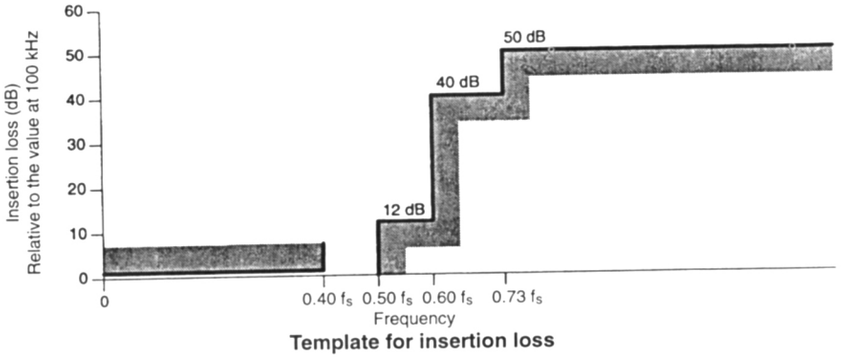
B.1 Figure B.1 depicts filter characteristics for pre- and post-filtering of Y', R', G', and B' component signals. Figure B.2 depicts filter characteristics for pre- and post-filtering of P'$_B$ and P'$_R$ component signals.

B.2 The passband frequency of the component Y', R', G', and B' signals is nominally 60 MHz for progressive systems and 30 MHz for interlaced systems.

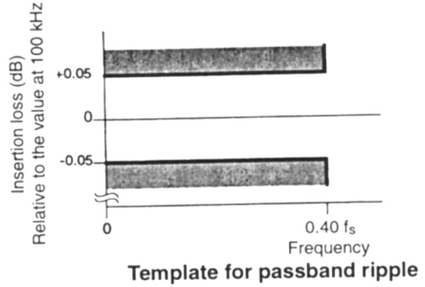
B.3 The value of the amplitude ripple tolerance in the passband is ± 0.05 dB relative to the insertion loss at 100 kHz.

B.4 The insertion loss characteristics of the filters are frequency-scaled from the characteristics of ITU-R BT.601. Insertion loss is 12 dB or more at half the sampling frequency of the Y', R', G', and B' components, and 6 dB or more at half the sampling frequency of the P'$_B$ and P'$_R$ components, relative to the insertion loss at 100 kHz.

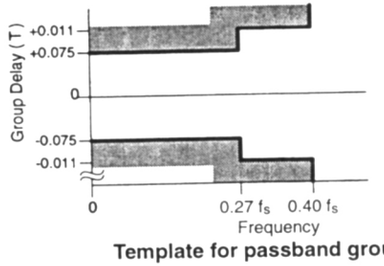
B.5 The specifications for group-delay in the filters are sufficiently tight to produce good performance while allowing the practical implementation of the filters.



Template for insertion loss



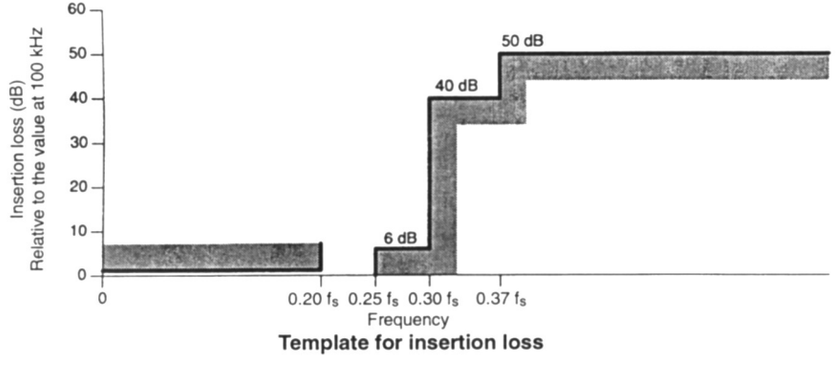
Template for passband ripple



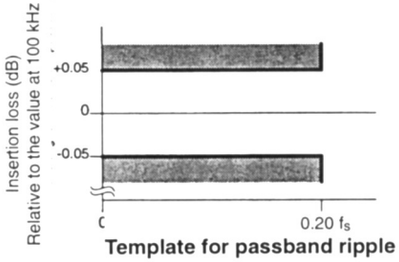
Template for passband group-delay

NOTE — The value of f_s is given in table 1.

Figure B.1 – Filter template for Y' and R'G'B' components

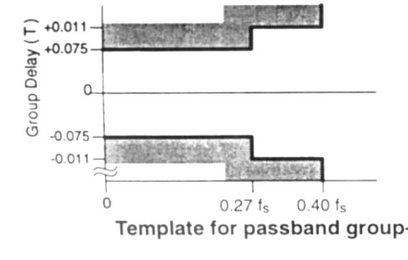


Template for insertion loss



Template for passband ripple

NOTE — The value of f_S is given in table 1.



Template for passband group-delay

Figure B.2 – Filter template for P'_B and P'_R components

Annex C (informative)
Production aperture

C.1 Production aperture

A production aperture for the studio digital signal defines an active picture area of 1920 pixels by 1080 lines produced by signal sources such as cameras, telecines, digital videotape recorders, and computer-generated pictures conforming to this standard.

C.2 Analog blanking tolerance

C.2.1 The duration of the maximum active analog video signal measured at the 50% points is standardized as 1920 clock periods. However, the analog blanking period may differ from equipment to equipment and the digital blanking may not coincide with the analog blanking in actual implementation.

C.2.2 To maximize the active video duration in picture origination sources, it is desirable to have analog blanking match digital blanking. However, recognizing the need for reasonable tolerance in implementation, analog blanking may be wider than digital blanking (see figure 3).

C.2.3 To accommodate a practical implementation of analog blanking within various studio equipments, a tolerance of six clock periods is provided at the start and end of active video. Accordingly, the analog tolerance to parameters b and e of table 5 are as follows:

Parameter	Definition	Nominal value (ref.clocks)	Tolerance (ref. clocks)
b	0_H to end of active video	2112	− 6 + 0
e	0_H to start of active video	192	− 0 + 6

C.2.4 The relationship of the associated analog representation (inclusive of this tolerance) with the production aperture is shown in figure 3.

C.3 Transient regions

C.3.1 This standard defines a picture aspect ratio of 16:9 with 1920 pixels per active line and 1080 active lines. However, digital processing and associated spatial filtering can produce various forms of "transient effects" at picture blanking edges and within adjacent active video that should be taken into account to allow practical implementation of the studio standard.

C.3.2 The following factors contribute to these effects:

– Bandwidth limitation of component analog signals (most noticeably, the ringing on color-difference signals);

– Analog filter implementation;

– Amplitude clipping of analog signals due to the finite dynamic range imposed by the quantization process;

– Use of digital blanking in repeated analog-digital-analog conversions; and

– Tolerance in analog blanking.

C.4 Clean aperture

C.4.1 The bandwidth limitation of an analog signal (pre- and post-filtering) can introduce transient ringing effects which intrude into the active picture area. Also, multiple digital blanking operations in an analog-digital-analog environment can increase transient ringing effects. Furthermore, cascaded spatial filtering and/or techniques for handling the horizontal and vertical edges of the picture (associated with complex digital processing in post-production) can introduce transient disturbances at the picture boundaries, both horizontally and vertically. It is not possible to impose any bounds on the number of cascaded digital processes which might be encountered in the practical post-production system. Hence, recognizing the reality of those picture edge transient effects, the definition of a system design guideline is introduced in the form of a subjectively artifact-free area, called clean aperture.

C.4.2 The clean aperture defines an area within which picture information is subjectively uncontaminated by all edge transient distortions. The clean aperture should be as wide as is needed to accommodate cascaded digital manipulations of the picture. Computer simulations have shown that a transient effect area defined by 16 samples on each side and 9 lines at both top and bottom within the digital production aperture, would represent an acceptable (and practical) worst-case level of protection in allowing two-dimensional transient ringing to settle below a subjectively acceptable level.

C.4.3 This gives rise to a clean aperture of 1888 horizontal active pixels by 1062 active lines whose quality is guaranteed for final release. The clean aperture lies within the production aperture as shown in figure C.1.

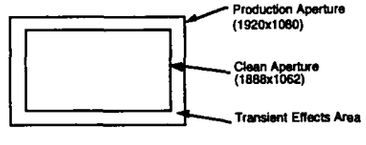


Figure C.1 – Clean aperture

Annex D (informative)
Bibliography

SMPTE RP 160M-1991, Three-Channel Parallel Analog Component High-Definition Video Interface

ITU-R BT.601-2, Encoding Parameters of Digital Television for Studios