Distribution, Routing, and Timing in a Digital Facility

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In previous articles, we have discussed the various digital signal types used in broadcast television, conversion between these different signals, and issues of quality control. This article discusses how to get digital signals around a television facility and addresses the issue of system timing.

Two types of distribution amplifiers are required in a serial digital television system: fan-out and equalizing/reclocking (Figs. 1a and 1b). Fan-out distribution amplifiers provide a non-loop through input and multiple nonreclocked outputs. The fan-out serial distribution amplifier can recover a signal after a cable run of up to 50 m and can be used between adjacent racks and in small systems. The cable run can be much longer if the signal is clean and free of jitter.

The equalizing/reclocking distribution amplifier can recover a signal after a cable run of over 200 m at 270 Mbits/sec. In addition to automatically restoring the correct signal level, this amplifier completely regenerates (reclocks) the serial data stream and provides new, clean pulses. The equalizing/reclocking distribution amplifier would be used in large facilities after long cable runs; the number of outputs will generally be the same as for the simple fan-out device.

Routing of Serial Signals

There are many potential benefits in using serial digital signals for routing in a television facility. The ability to multiplex or embed AES digital audio signals into the serial bit stream allows the switching of video and audio signals to be performed on a single level of a matrix — this is great for switching in television network centers. Also, in digital television, we can switch component (4:2:2) signals in a single level of a matrix. (Of course, we can alternatively switch composite [$4f_{sc}$] signals on a single level.) Remember that in the analog domain, you need one level for composite video and three levels for Y, R-Y, and B-Y. In analog switching, you also need separate levels for each channel of audio. In both digital and analog routers, a remote control panel can be configured to switch many levels simultaneously.

Digital routers generally incorporate input processing features not found in analog routers. These features may include input equalization and reclocking, as well as automatic timing of the input signal. It is possible to use a wideband analog router for some serial signals. A 100-MHz analog router can have sufficient bandwidth for the serial data stream of a $4f_{sc}$, 143 Mbit/sec signal. But at higher rates (270 Mbits/sec, for instance), the switcher must emulate the effects of coaxial cable ($1/\sqrt{}$ frequency). We must also be aware that an analog router will not provide a clean serial switch between two signals. A digital router should operate at all required serial data rates and can be designed to provide a clean switch between two synchronous and timed signals.

It is important to note that, if signals are not perfectly timed, a timing buffer is generally needed somewhere in the system to ensure that the switching operation is clean. This is especially true if the signal is carrying embedded audio, which may be susceptible to audible disturbances. To solve these problems, some manufacturers offer special "clean switch" routers. These routers ensure glitch-free switching between two inputs by buffering the outputs between two different buses.

Timing in the Digital Domain

As in analog systems, digital video signals must be synchronous and timed. The job of timing digital systems will be easier in digital systems because it is possible to provide auto timed inputs on switching/mixing devices. In analog systems we usually have to compensate for increments in nanoseconds and, on occasion in larger systems, in microseconds. Larger timing differences, found in analog systems, have generally been created

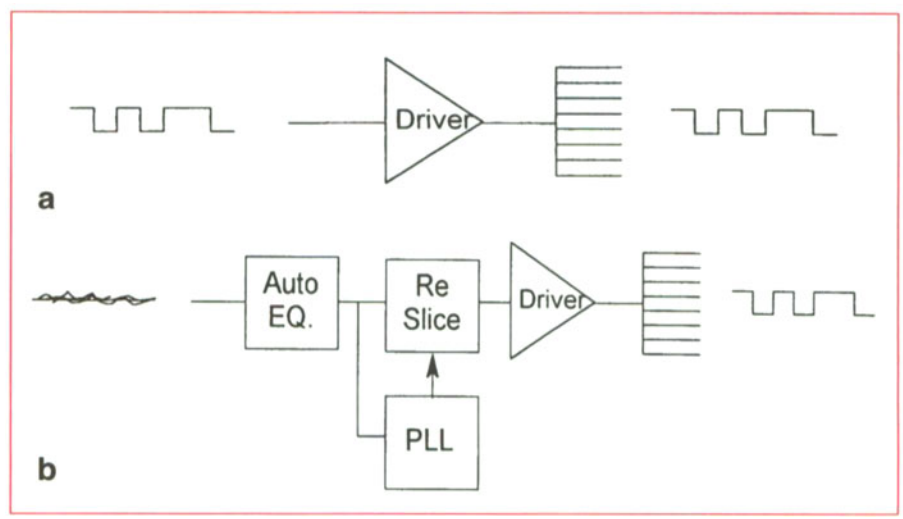

Figure 1. Two types of distribution amplifiers in a serial digital TV system: (a) fan-out and nonreclocking; (b) equalizing and reclocking.

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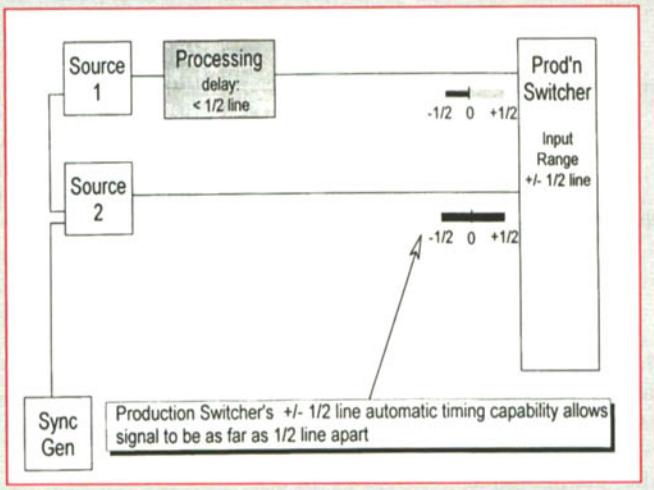

Figure 2. Automatic timed inputs (case no.1).

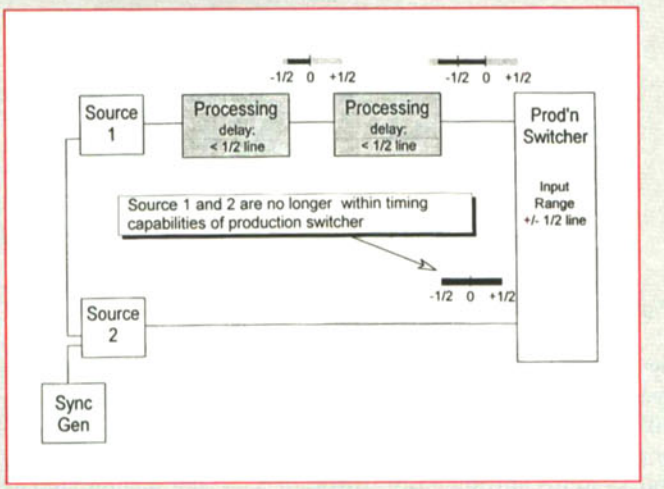

Figure 3. Reaching limit of timing compensation.

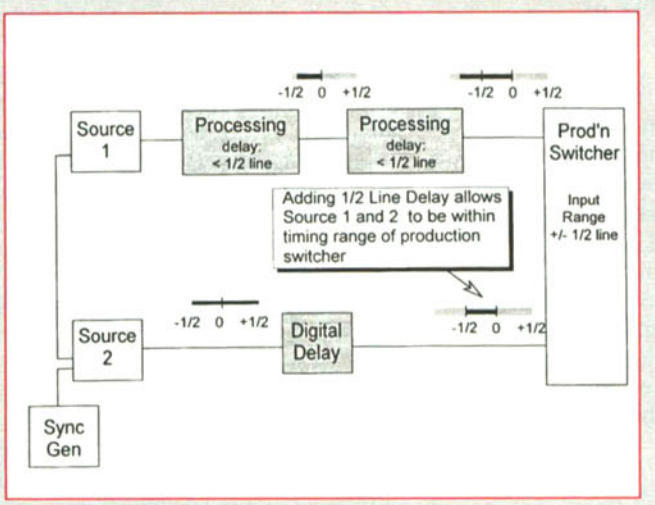

Figure 4. Solution 1: add digital delay.

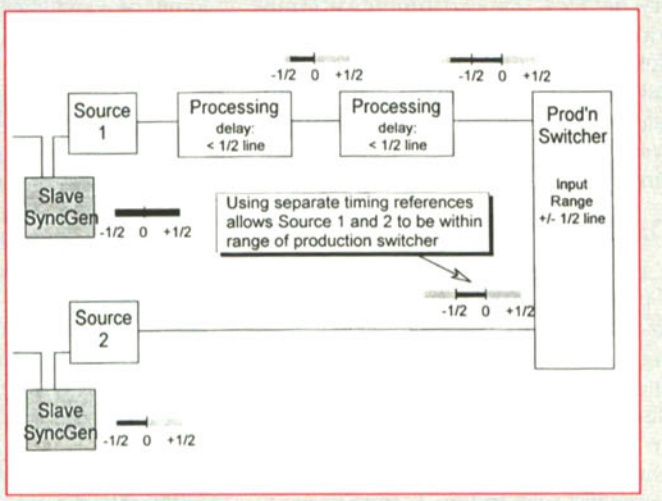

Figure 5. Solution 2: independent slave sync generators.

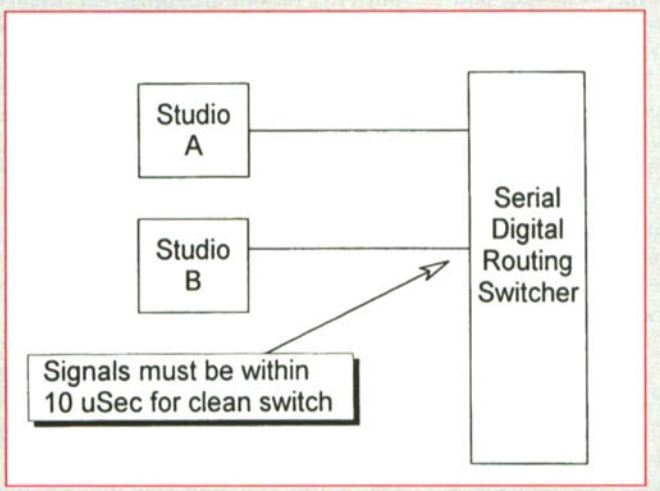

Figure 6. Devices without timing compensation.

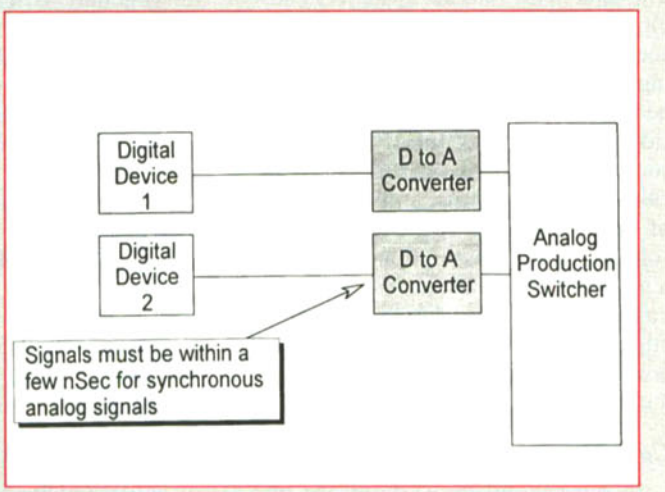

Figure 7. Timing inputs to D/A converters (case no. 3).

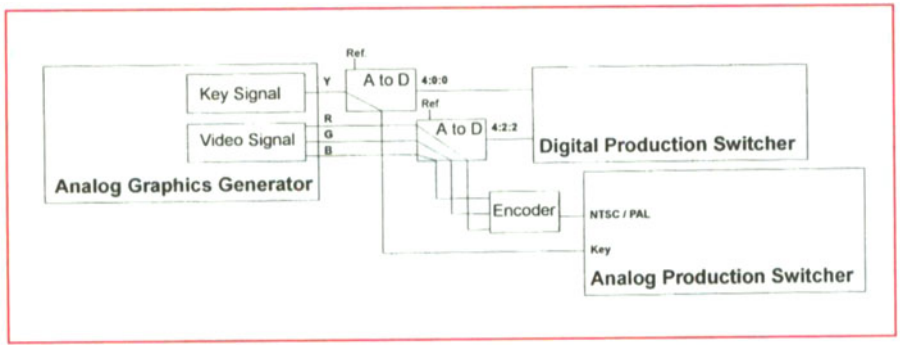

Figure 8. Timing considerations (case no. 4).

by some digital device such as a frame synchronizer. This can result in timing differences of a many TV lines, fields, or frames (many milliseconds). In digital systems, propagation through a device can take much longer due to data storage in latches and other memory devices. Typical timing differentials are in the order of lines and fields/frames. What is great about digital systems is that inputs can be automatically timed, thereby simplifying system setup. Let's consider five different timing scenarios.

Case No. 1

Figure 2 shows two sources feeding a production switcher. One of the sources is being processed and is arriving at the switcher less than one-half line later than the other source. In this case, the production switcher has plus or minus one-half line of automatic timing compensation and everything works just fine. In Fig. 3, more processing is carried out on the first source. The total delay into the switcher is now close to one line compared with the second source. The automatic timing input cannot compensate for this delay because it is too large. The first solution (Fig. 4) is to delay the second source, using a digital delay line. In this case, somewhere close to one-half line of delay would be sufficient. Another solution (Fig. 5) is to time each problem source with a slave sync generator capable of providing large timing adjustments. In serial systems, analog color black is still distributed to provide a master genlocking source.

Case No. 2

In the second case, there are two studios in a facility that are synchronous and feeding a routing switcher in master control. As long as the serial signals are within about 10 μsec, a "clean" switch will take place. This is quite a difference, because when timing analog signals, the analog signals must be within a degree of subcarrier or a couple of nanoseconds at the input of a switcher (Fig. 6).

Case No. 3

In the third case, two synchronous digital devices are feeding digital-to-analog converters ahead of a switcher. If we assume that the digital-to-analog (D/A) converters have the same progagation path, then the inputs to the D/A converters must be timed to a degree of subcarrier or a couple of nanoseconds. This means that the timing ability of the digital devices or D/As must have a fine timing resolution to regulate the signals in the analog domain (Fig. 7).

Case No. 4

In the fourth case, an analog character generator is feeding an analog and a digital production switcher (Fig. 8). There are several timing considerations in a situation like this. The key signal must be delayed into the analog production switcher to compensate for the encoder. When the key and RGB fill signals are converted to digital, there will be a delay in the key path. One must also look at the timing of the analog key signal relative to its sync. When digitized, if there are any differences, these will be seen in the digital domain.

The RGB-to-sync timing should be checked, as well. If an external reference is being used to generate the start of active video (SAV) code sequence at the analog to digital conversion, the relative timing between the external reference and the video signal must be checked. In other words, the input video (not sync) must be timed to the external reference input. If the digitized key and fill signals are externally referenced during the conversion process and there is a difference between the external sync and video or key, an incorrect picture position will result.

Remember that autotiming at the input to a digital switcher is done using the SAV. The digital switcher will autotime using SAV derived from the sync at the conversion. Any differences in picture position will be seen at the output of the digital switcher.

Case No. 5

We should not overlook timing considerations when converting from digital back to the composite analog domain. NTSC requires a 4-field sequence, and PAL needs 8 fields, before the same patterns of sync and subcarrier relationships are repeated. This timing information is not available in the component digital or analog world, so we have to provide it to the encoder in the form of a genlocking color black (black burst) analog signal. Here lies the problem. In order for the digital signal to be able to make use of the analog reference signal, the two have to be timed together. The amount of timing difference that can tolerated depends upon the amount of video storage that is available in the encoder. The safest solution is to use an encoder with a 2-field buffer. The output signal can then be timed to whatever is desired. Encoders need at least a small buffer to absorb any residual jitter in the digital signal before it is converted to analog. Some economies may be realized in an encoder by using a small buffer of perhaps only one or two lines. In this case, it is important to provide a correctly timed reference.

Conclusion

Although digital devices have longer propagation paths, timing digital systems can be much easier if autotimed inputs to switchers are available. In the next tutorial we will discuss a real-world situation showing the evolution of a facility from analog to hybrid, and finally to digital.