Second Generation HDTV Switcher

By Vince Harradine and Alan Turner

High-definition television systems were first shown at the International Broadcast Convention, Brighton, U.K., in the early 1980s but have since had only limited impact in specialist areas due to the size, weight, and consequential cost of high-definition processing, storage, and transmission. In Japan today at least 12 hours of high-definition material are broadcast per day to more than one-half million receivers using a compression technology known as multiple sub-Nyquist encoding or MUSE. There is now a growing demand from Japanese broadcasters and program producers to capture their original material using high-definition systems. Sony is responding by introducing a new generation of high-definition products. The range of products includes studio cameras, portable cameras, studio videotape recorders (VTRs), portable VTRs, digital multi effects, and digital switchers all suitable for live, production, and post-production use.

During 1992 to 1993 the R&D department of Sony Broadcast & Professional Europe developed prototype hardware for a 2ME+DSK (mix effect + downstream keyer) high-definition (HD) digital video switcher with a specification similar to that of the 525/625 DVS-6000C product.

The video inputs and outputs of that development conformed to the SMPTE 260M standard that defines the digital representation and bit-parallel interface for 1125/60 HD production systems. Therefore, the HD digital switcher processed digital video based on the three primary signals E_G', E_B', and E_R' that are transmitted at the 22:22:22 level of the CCIR digital hierarchy with a nominal sampling frequency of 74.25 MHz and 10 bits/sample. Additionally, the standard also defines that the parallel interface uses a 93-pin connector and connecting cable consisting of 31 shielded conductor pairs.

Extensive reuse was made of application specific integrated circuits (ASICs) originally developed for the 525/625 DVS-8000C digital switcher. These ASICs had been designed for operation nominally at 4 f_{sc} phase-alternation line (PAL; 17.734 MHz), and therefore the HD digital switcher processor was designed to operate with one-quarter rate HD data (18.5625 MHz). Based on these conditions, the processing electronics of the prototype HD digital switcher occupied a 7 x 10 U chassis with more than 75 chassis-to-chassis video data interconnecting cables. Such a product would have been prohibitive in space-conscious applications such as outside broadcast vehicles.

To meet with the introduction of Sony's next generation of HD equipment suitable for live, production, and post-production use, the R&D group is now developing a preproduction HD digital switcher. The experiences gained during the previous development have been vital to achieving the primary product objectives—a 30-input 3ME HD digital switcher with a specification similar to that of the current 525/625 DVS-7000C product, but occupying just a single 15 U chassis.

Extensive and innovative work at the system design phase has produced a product design that is small, low-power, low-cost, and flexible. This has been achieved primarily in three ways:

- By using newly developed HD serial digital interface technology
- By reevaluating ASIC function and extending bandwidth to allow video data processing at a clock speed of 74.25 MHz
- By developing a low-power solution to the transfer of video data internally at the full HD data rate.

The focus of this paper will be on our investigation into reliable board-to-board communications at a data rate of 74.25 Msamples/sec.

HD Digital Switcher Key Features

- All input-output (I/O) is to be HD serial digital interface (SDI)
- 30 primary inputs
- Automatic input timing
- 15 external outputs including ME 1 Program, ME 2 Program, Program, PVW-Preview, Clean, and 10 Auxilary busses
- Color black and 2 color backgrounds (1 with wash capability)
- YC_bC_r 10-bit processing (internally conforms to SMPTE 260M)
- 3ME multilevel structure
- ME reentry
- 2 key processors per ME
- Each key processor has border, drop border, drop shadow, and outline
- Key source and fill fed from primary inputs
- 1 chroma-key channel per ME
- Processor amp controls for all ME backgrounds and key fills
- Mix, non-additive mix (NAM), and super mix modes
- 1 wipe generator per ME
- 1035/1080 active line operation
- 59.94/60-Hz switchable operation
- 16:9/4:3 switchable operation
- Frame memory system
- Fully functional and assignable color corrector
- Signal processor to occupy 1 x 15 U chassis
- Digital Multi-Effects (DME) Link supported
- RS-422 editor interface

System Input/Output

Although ratified as part of the

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SMPTE 260M standard, the 93-pin interconnect system for bit parallel interface of HD data has not been accepted by the limited number of HD equipment manufacturers. This is due to a number of reasons and in particular its physical size, cost, and potential unreliability.

Remember the early days of ITU-R 656 interconnects where the original standard defined the use of the slide/lock connection for those awful 25-way D-Sub connectors? Many installations did in fact make use of the parallel digital interface for ITU-R 656, but it was not until the advent of the SDI as defined in SMPTE 259M that digital system installations really took off in a big way.

Since 1993, the development group of Sony's Broadcast division has been working on a HD version of the serial digital interface (HD SDI). The result of this work is a chipset suitable for the transmission of full bandwidth 10-bit luminance (Y) and color difference (C_bC_r) video data over a regular coaxial cable at a data rate of 1.485 Gbits/sec.

The HD SDI technology is available as a two-circuit board set, one for transmitting the other for receiving. Each of the two circuit boards measures 100 x 70 mm with the HD SDI connection being made via a subminiature RF connector type-A (SMA) radio frequency (RF) connector. The parallel 74.25 MHz Y and multiplexed C_bC_r data are input and output via a low-profile 100-pin surface mount connector.

The key enabling technology for the HD SDI is a gallium arsenide (GaAs) ASIC that performs the serial-to-parallel/parallel-to-serial conversion. This ASIC is housed in a 124-pin package incorporating a three-metal fin heatsink.

This HD SDI technology is now generally available and is being used by a large number of manufacturers developing HD products for the Japanese market. Indeed all of the next generation of Sony HD products currently under development will make use of this HD SDI technology with the HD digital switcher being no exception.

As can be seen from the above feature list, the system supports up to 30 primary inputs, 15 outputs including 10 aux outputs. This has only been made possible by using the HD SDI boards thus allowing the system to occupy only a single 15 U chassis. The 2 input boards of the HD digital switcher each house 15 of the HD SDI input modules with the output board similarly housing 15 of the HD SDI output boards. Once the input video data has been deserialized, subsequent processing is on the 10-bit parallel data bus at 74.25 Msamples/sec.

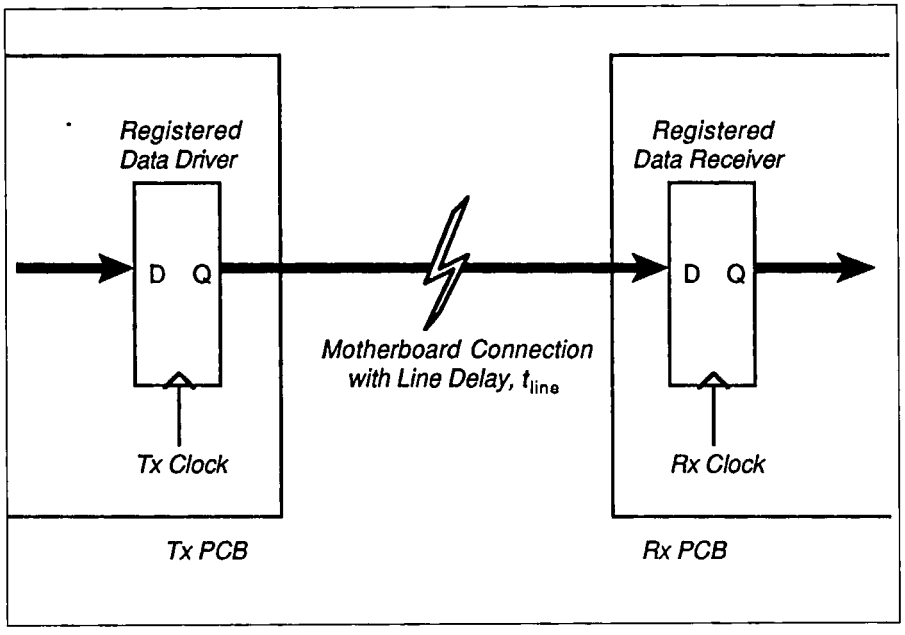

Figure 1. Synchronous data transmission between Tx and Rx boards along the motherboard.

An important ASIC that has been developed for the new switcher is the so-called I/O processor. This device comprises a full HD line first-in first-out (FIFO) that can be operated in both synchronous and asynchronous modes making it suitable, for example, as the input line synchronizer. In addition, this ASIC provides all commonly required I/O processing functions such as:

- End-of-active video/start-of-active video (EAV/SAV) detection and correction of single bit errors in the timing reference signal (TRS) word.
- FIFO write reset generated from input SAV words.
- Black and white hard and soft variable clipping.
- Hard and soft blanking insertion.
- EAV/SAV insertion.
- Delay/line delay function.

This very useful ASIC has been developed for operation at 74.25 MHz using a 0.5-μm technology and is housed in a 68-pin PLCC package.

The HD System Design Challenge

When designing large digital video processing systems whose I/O conforms to, for example, ITU-R 601, such a system will typically consist of a number of individual daughter printed circuit boards (PCBs) that plug into and communicate with one another using a motherboard. In a ITU-R 601–based system, the processing speed of the video data will be dependent on whether processing is on demultiplexed Y and C_bC_r data, in which case the speed is 13.5 MHz per data path, or multiplexed C_bYC_rY data, where the frequency of operation is 27 MHz.

Generally, such systems are designed to be synchronous with a single master clock. The master clock will drive every board in the system providing a data-only channel between cards. Subsequently, data transfers between PCBs must complete within the clock period of either 74 or 37 nsec. Although one must be careful when designing at such speeds, issues such as propag, or even extender boards (used during testing) are rarely considered. However, in designing a system to allow video data processing and board-to-board data communications to operate within the full HD clock period of 13.468 nsec, these are

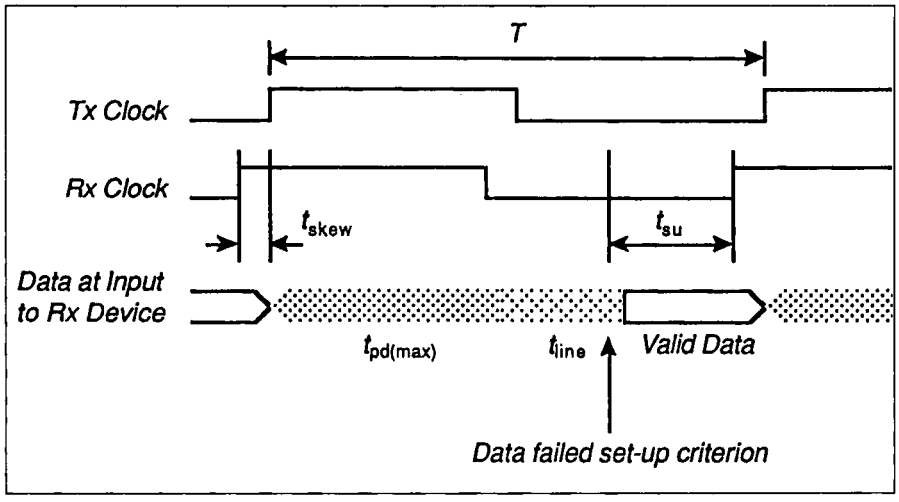

Figure 2. Clock skew causes problems meeting Rx device data setup time.

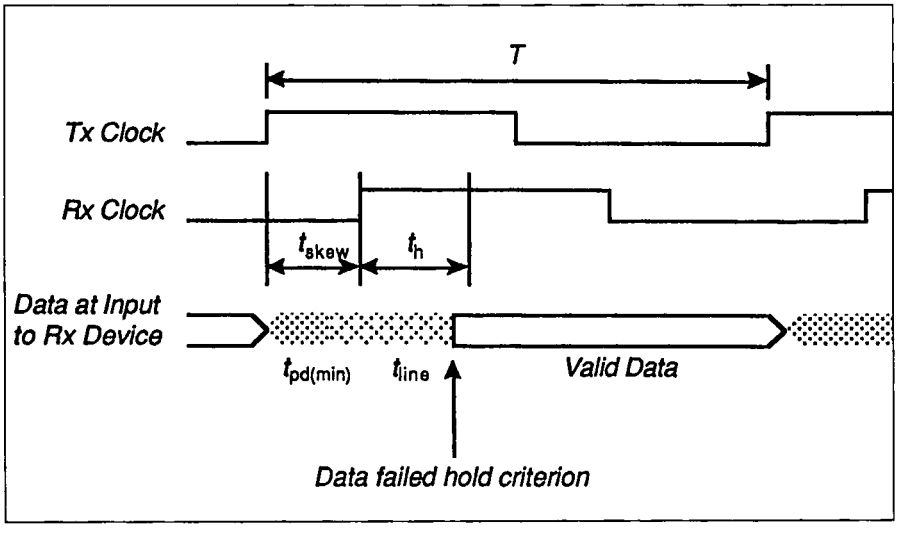

Figure 3. Clock skew causes problems meeting Rx device data hold time.

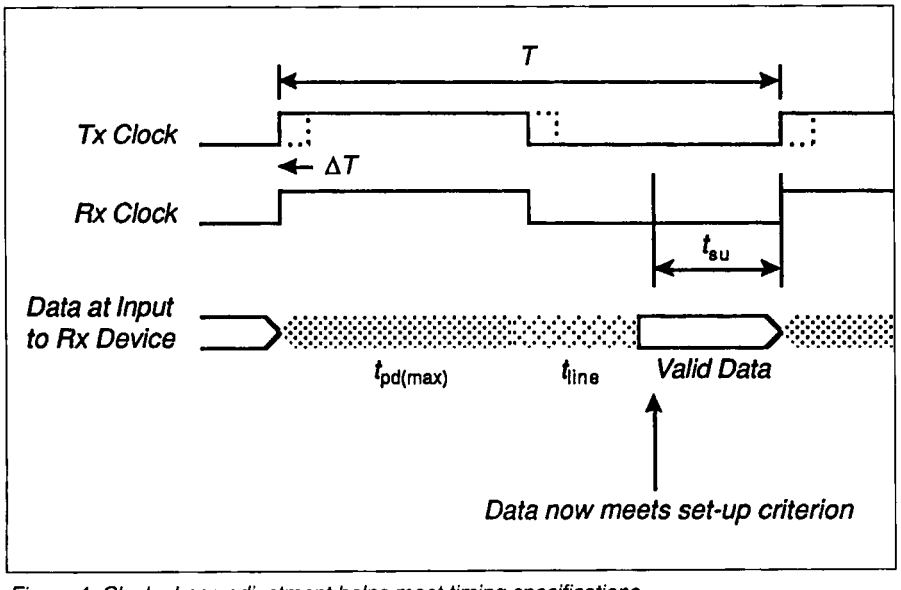

Figure 4. Clock phase adjustment helps meet timing specifications.

factors that now have to be taken into account.

An alternative approach to synchronous data transfers is to use a completely asynchronous solution where the transmit clock is also sent with its data bus to the receiver. At the receiver the data is synchronized to the local board clock in a FIFO memory.

A major part of the new switcher system design involved investigating solutions to the problems of clock distribution and board-to-board data transfers. These are serious problems, considering that the majority of processing is at the full HD rate of 74.25 MHz, including board-to-board data transfers.

Synchronous Data Transfer Approach

First, the synchronous data transfer timing (Fig. 1) will be analyzed to determine the constraints placed on component choice and system design.

Next, techniques to improve operating margins will be considered and the effect on the timing of the data transfer analyzed.

Finally, a comparison of emitter coupled logic (ECL) and transistor-transistor logic (TTL) implementations is made.

Basic Analysis

Clock skew and interboard delay are the factors that ultimately set the maximum data transfer rate as both erode the fundamental clock cycle time available. Ideally there should be zero phase error between clocks across all daughter PCBs.

It is possible to optimize the clock distribution for minimum skew as we are dealing with only a few signals. However, for the data, the variation in distances between daughter PCBs means that skew is unavoidable. This is not a problem provided that the transfer with the longest delay (PCBs furthest away from each other) can be completed in the cycle time. Delays are kept to a minimum by limiting this distance and using registers with low propagation delay.

The speed at which a motherboard data transmission scheme will operate is determined by:

- System clock period, T.
- Transmit and receive device parameters; setup time, t_{su}, hold time, t_h,

clock skew, t_{skew}, and minimum and maximum propagation delay, t_{pd}.

- Physical separation of the transmitting (Tx) and receiving (Rx) PCBs causing a transmission line delay, tline.
- Other physical characteristics (such as variation in PCB dielectric constant, mechanical track tolerances, connector boundaries, etc.) largely of minor significance.

Transmit and receive clocks will be skewed creating problems in meeting both the se-tup and hold times of the Rx data receiver (Figs. 2 and 3). Referring to Fig. 2 with a negative value of t_{skew}, data at the receiving device will meet the set-up time if:

$$T > t_{su} + t_{pd(max)} + t_{line} - t_{skew} \quad (1)$$

and, from Fig. 3, it will meet the hold time if

$$t_{skew} + t_h < t_{pd(min)} + t_{line} \quad (2)$$

Clock Phase Adjustment

In a high-speed digital system (>50 MHz) such as the HD digital switcher, clock phase adjustment may be necessary to accommodate excessively large or small line delays and thus meet the setup and hold requirements (Fig. 4). This adjustment may be achieved by using either phase-locked loops with output phase adjustment, delay line devices in the clock path, or possibly a combination of the two. Adjustment such as this, coupled with suitable bus interface devices, makes it possible to extend the bandwidth of a TTL system to full rate HD video data.

A graphical representation of how clock phase adjustment can ease the timing constraints set out in Eqs. 1 and 2 is shown in Fig. 5. For zero clock phase adjustment ($\Delta T = 0$) successful data transfer takes place only if the line delay between Tx and Rx devices lies in the range $C2 < t_{line} < C1$. However, by retarding or advancing the transmit clock by ΔT, the effect of a long, or short, line delay can be respectively reduced thus bringing the data timing into the region of operation.

$$C1 = T - t_{skew} - t_{su} - t_{pd(min)} \quad (3)$$

$$C2 = t_{skew} + t_h - t_{pd(min)} \quad (4)$$

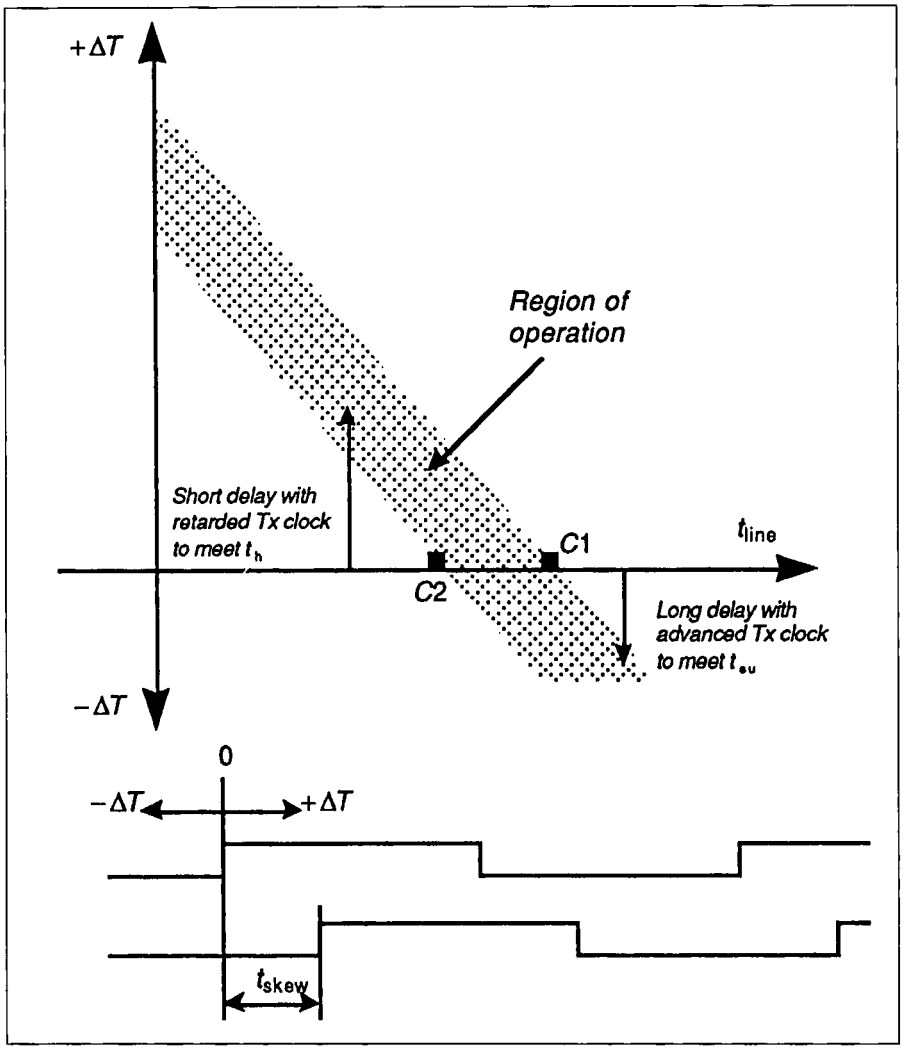

Figure 5. Operating region for data transfer employing clock phase adjustment.

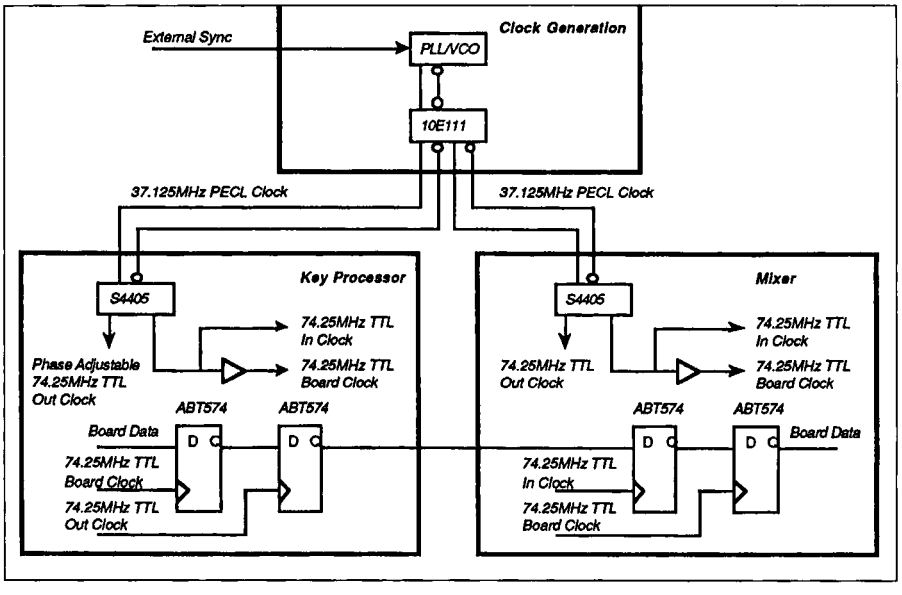

Figure 6. Board-to-board data transfer—the TTL solution.

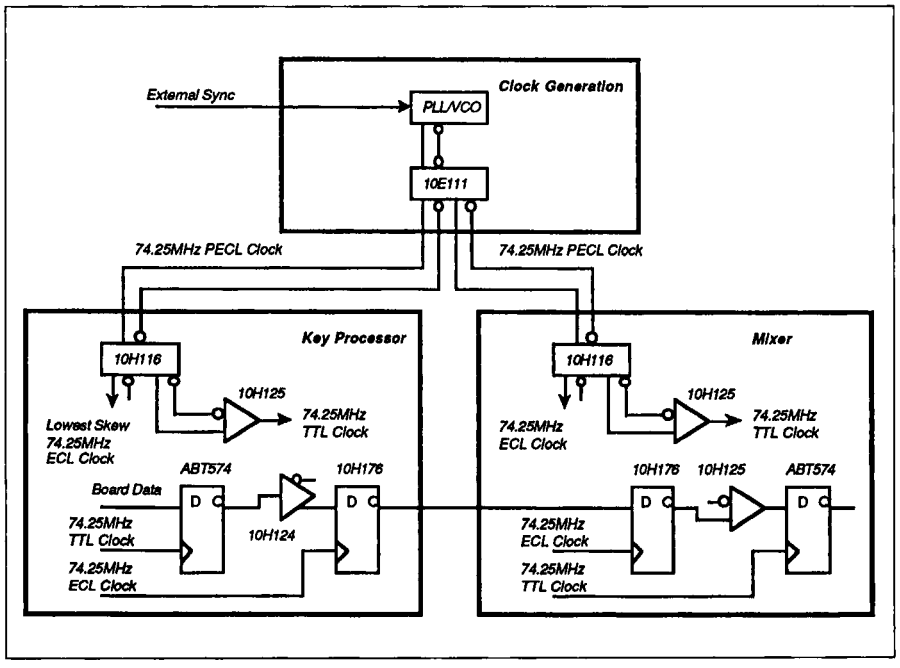

Figure 7. Board-to-board data transfer—the ECL solution.

Margin of Operation

The margin of operation (size of the operating region) can be calculated by combining Eqs. 3 and 4:

$$Margin = C1 - C2 = T - (2x\ t_{skew}) - t_{su} - t_h - t_{pd(max)} + t_{pd(min)} \quad (5)$$

if and only if the following criterion is met:

$$t_{pd(min)} < t_{skew} + t_h \quad (6)$$

i.e., C2 > 0 in Fig. 5.

If Eq. 6 is not met, all Tx clocks must be advanced, regardless of transmission distance (i.e., for all values of line delay).

Whatever scheme is used for clock phase adjustment (e.g., phase-locked loops, tapped delay lines, etc.), there will almost certainly be a minimum phase adjustment increment, ΔT_{min}. Clearly, a compensating phase adjustment must be able to bring a nonoperational data transfer into the operational region. Hence:

$$Margin > \Delta\ T_{min} \quad (7)$$

TTL vs. ECL Implementation

Using the above analysis it is possible to compare full rate data distribution using TTL with an ECL approach to demonstrate the good reasons for choosing an advanced TTL solution. Figures 6 and 7 illustrate examples of TTL and ECL solutions to the synchronous data transfer that can be analyzed using the above criterion. In addition other factors such as power consumption and PCB real estate used can be and are taken into account. Table 1 shows the main results of the TTL/ECL comparison.

Since both solutions meet with the stringent timing criteria, the main differences between technologies are power and size. TTL consumes 92% less power in the board-to-board data transfer circuitry than ECL and takes up over 73% less board space.

The use of ECL components places a heavy bearing on the power dissipation of individual circuit boards. In the digital switcher the mixer board with some eleven 10-bit video bus connections and six 12-bit key bus connections, ECL data buffering will consume over 79 W compared with 6 W for TTL buffering. This high-power dissipation arises largely due to the high static power dissipation of the ECL parts, as well as dissipation in the necessary termination resistors.

Asynchronous Data Transfer Approach

In this section, the improvement in operating margins due to adopting an asynchronous data transfer approach (Fig. 8), instead of a synchronous technique, will be analyzed. Some consideration will then be given to the practical aspects of such a system.

Basic Analysis

Using Eqs. 1 and 2 from the basic analysis of the synchronous data transfer, it can be shown that the asynchronous approach increases the margin for setup time, t_{su}, and hold time, t_h.

From Eq. 1 as $t_{skew} = t_{line}$ then data at the receiving FIFO will meet the set-up time provided:

$$T > t_{pd(max)} + t_{su} \quad (8)$$

Similarly from Eq. 2, as $t_{skew} = t_{line}$ then the hold time requirement at the receiving FIFO will be met if:

$$t_{pd(min)} > t_h \quad (9)$$

Table 1 — Main Findings of TTL vs. ECL

Criterion	TTL	ECL
Interface I/O power consumption	34 mW/bit	435 mW/bit
Clock buffering power consumption	124 mW/clock	158 mW/clock
Timing margin of operation	3.5 nsec	7 nsec
Crosstalk (edge rate of change)	1 V/nsec	0.8 V/nsec
Interface I/O board area	0.025 sq. in./bit	0.094 sq. in./bit
Clock buffering board area	0.105 sq. in./clock	0.131 sq. in./clock
Interface I/O cost	$0.32/bit	$2.18/bit
Clock buffering I/O cost	$5.89/clock	$1.22/clock

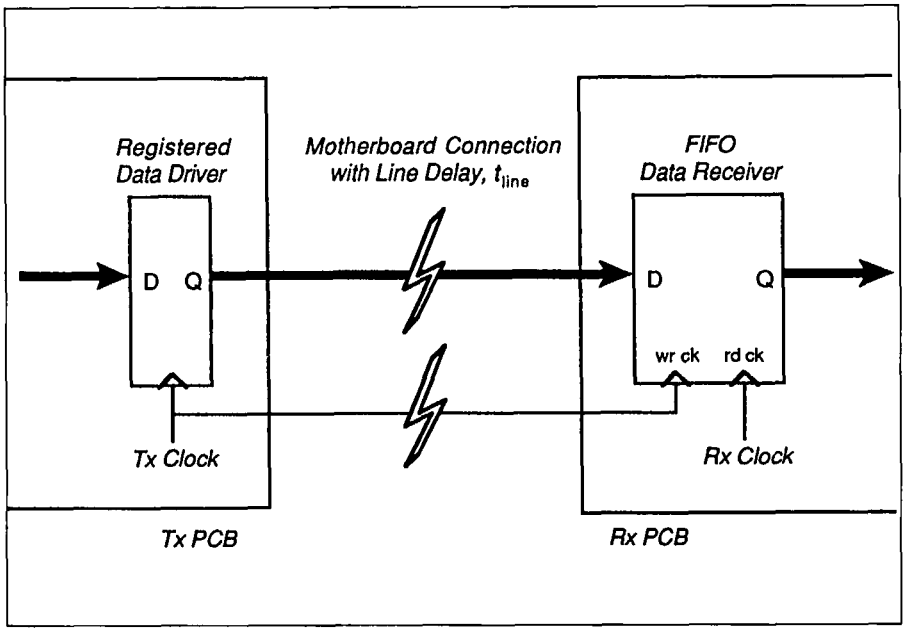

Figure 8. Asynchronous data transmission between Tx and Rx boards along the motherboard.

This clearly increases the margin to allow reliable data transfer by effectively removing the variables t_{skew} and t_{line}.

Other Considerations

- The same arguments regarding TTL versus ECL implementation equally applies to the asynchronous approach.
- The data bus together with its associated transmit clock must follow the same path on the motherboard.
- Additional overhead of requiring receive FIFO for resynchronization.
- Potential increase in crosstalk due to transmit clock with every data, particularly significant in the HD digital switcher.

Conclusion

With adequate devices to satisfy the timing criteria of the synchronous approach, as would be expected, TTL looks to be the best implementation when dealing with many video data buses.

However, considering the critical timing requirements, such a system is judged to be impractical to implement in mass-produced equipment. Also, there would be concern over data transfer reliability during test and debug, where it is necessary to use extender boards.

Consequently an asynchronous data transfer approach has been adopted for the HD digital switcher. The advantages of this being:

- Relaxed timing tolerances for board-to-board data transfer
- Removal of the need for tight control otherwise placed on a centrally distributed clock

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THE AUTHORS

Vince Harradine is an R&D Project Manager in the R&D department of Sony Broadcast & Professional Europe and is responsible for the High Definition Switcher, High Definition Digital Multi Effects, and DNE-50 Portable Edit Controller projects. He joined the department in 1979 as a technician during the early days of digital VTR development. He graduated in 1985 with a degree in electrical and electronic engineering, and since then has worked on a variety of projects including the D-1 DVTR, motion compensated standards conversion, digital color correction (BVX-D10), high-definition digital signal processing systems, nonlinear editing, newsroom computer, and journalist workstation systems. A member of the SMPTE, he holds more than ten patents and has published several papers in related project areas.

Alan Turner is a Principal R&D Engineer in the R&D department of Sony Broadcast & Professional Europe and is the project leader of the High Definition Digital Multi Effects project. He graduated from the University of Surrey in 1986 with a degree in electrical and electronic engineering; this included a year with Sony's R&D department gaining valuable experience in digital video processing, including exposure to HDTV. After graduation, he joined the BBC Designs Department to work on diverse projects including digital audio synchronization, band II radio microphone systems, and telecine control. In 1988, he returned to Sony, and since then he has worked on several video processing projects including real-time slow-motion replay, the Betacam SX compression chip set, HD-to-525 down converter IC, and HD DME systems.