

### 1. General

scope. This standard defines the electrical and mechanical characteristics of an interface comprised of a general purpose communication channel and interface device(s) used for transfer of data and digital control signals in equipment utilized in the production, production, and/or transmission of visual information. It is intended that the communication channel and device(s) described in this standard be part of an overall equipment system, allowing interconnection of programmable and nonprogrammable control and access equipment as required to configure an operational system with a defined function. The standard is also intended to allow rapid reconstruction of a system providing more than one function utilizing a given group of equipment.

The electrical and mechanical specifications set forth in this standard are intended for use in both fixed plant and field operational environments. These specifications take into account the requirement to function reliably without causing undue interference with other signals normally found in these environments.

This standard defines the electrical and mechanical characteristics of the communication channel and the associated interface device(s), to include design specifications, performance requirements, safety requirements, and the communication protocol used in or by such equipment.

The primary intent of this standard is to define an electrical and mechanical interface for a communication channel for the purpose of

interconnecting equipment by external means. This standard, or sections thereof, may be applied to the interconnection of elements within an item of equipment.

**1.2 Definitions.** For the purposes of this standard, the following definitions shall apply:

Equipment means either a single device which connects to the interface system or a group of interconnected devices, providing a specified operational function, having one common connection to the interface system.

Interface Bus refers to the communication channel.

**1.3 Object.** The intent of this standard is to:

Define a general-purpose interface system for use in the environment specified in 1.1

Specify equipment-independent electrical, mechanical, and functional interface characteristics which permit equipment to connect and communicate unambiguously via the interface system

Specify terminology and definitions related to the electrical and mechanical portion of the interface system

Enable the interconnection of independently manufactured equipment into a single functional system

Permit equipment with a wide range of operational capabilities to be connected to the interface system simultaneously

Define a system which is user configurable

Define a system based on readily obtainable standard components

#### 1.4 Interface System Overview

**1.4.1** This standard applies to systems, or portions of systems, which have the following characteristics:

A full-duplex four-wire communications channel is utilized

A nominal maximum bus length of 1220 m (4003 ft)

Data is transmitted asynchronously, bit serial, word serial

Standard transmission rate on the interface bus is 38.4 kilobits per second (kb/s)

Data exchange between devices is digital (as distinct from analog)

**1.4.2** The function of the interface system is to provide an effective communications link over which messages are carried in an unambiguous way among a group of interconnected devices.

**1.4.3** The interface system described in this standard assigns one of two operational characteristics to all devices:

**Bus Controller.** Each interface system contains one bus controller which supervises all tributaries in the system. This supervision is exercised through the use of interface protocol. The bus controller may also perform one or more functions in the operational plant in addition to its interface supervision. Although only one bus controller may be part of any particular interface system, it is recognized that an operational plant may make use of more than one interface system.

**Tributary.** A tributary transfers messages to and from an operational device via the interface system as specified in the interface system protocol. A tributary communicates messages through the interface bus only via the bus controller.

**1.4.4** The basic message paths and the bus structure shall be as follows:

The basic message path utilizes asynchronous, bit serial/word serial transmission via a balanced wire pair

The interface bus may be utilized in either point-to-point or multi-point configuration including but not limited to

A point-to-point bus connecting to a single bus controller

A multipoint bus connecting to a single bus controller

The interface bus is a four-wire bus which will effect two-way communication; separate wire pair for each direction; communication between devices is accomplished through the bus controller

**1.4.5** The data word and bus length are defined by the interface system specification

The standard serial data word is 8 bits; the bit data word is 10 bits; the complete serial data word consists of one start bit (SPACE), eight data bits (BYTE), a parity bit (EVEN), and one stop bit (MARK).

A BREAK character, comprising two consecutive SPACE characters, is used to synchronize all devices connected to the interface bus.

### 2. Electrical Characteristics

**2.1 Interface Circuit.** The basic electrical interface circuit is shown in Figure 1. It consists of three parts: the generator, the balanced interconnecting cable, and the load. The load may consist of one or more devices. An optional cable termination network may be used. The electrical characteristics of the generator and receiver are specified in terms of open-circuit voltage measurements while the interconnecting cable is specified in terms of its electrical characteristics.

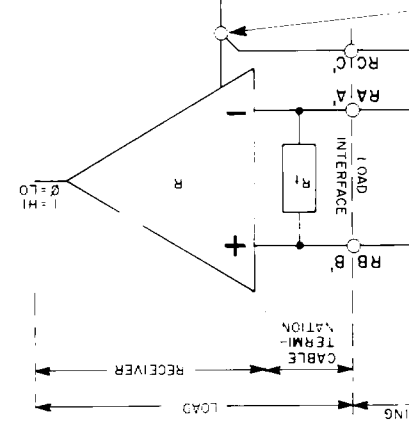
**2.2 Generator Characteristics.** The generator shall have characteristics of the generator circuit in accordance with measurement methods specified through 2.2.6 and illustrated in Figure 2. The generator circuit meeting these requirements results in a low impedance (100 ohms) balanced voltage source producing a peak-to-peak voltage applied to the interconnecting cable in the range of 2 to 6 volts. The maximum voltages appearing across the interconnecting cable are defined as follows:

The test termination measurement shall be made with a test load of two resistors, 50 ohm = 1%, connected in series between the generator output terminals as shown in Fig. 2b. The results of this measurement shall be as follows:  
 The magnitude of the differential voltage ( $V_t$ ) measured between the two output terminals shall not be less than either 2.0 volts or 50% of the magnitude of  $V_o$ , whichever is greater. For the opposite binary state the polarity of  $V_t$  shall be reversed.

**2.2.2** The test termination measurement shall be made in accordance with Fig. 2b.

of this measurement shall be as follows:  
 The magnitude of the differential voltage ( $V_o$ ) between the two generator output terminals shall not be more than 6.0 volts.  
 The magnitude of the voltage between either of the two output terminals and generator output terminals shall not be more than 6.0 volts.

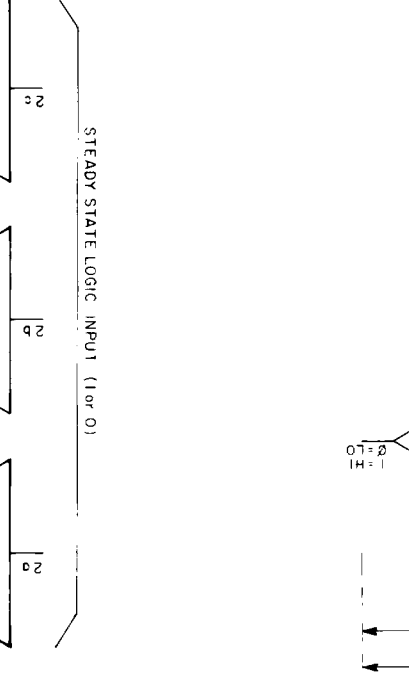
**Fig. 1**  
 Balanced Digital Interface Circuit



The B terminal of the generator shall be negative with respect to the A terminal for a binary 0 (SPACE) state.  
 The A terminal for a binary 1

The magnitude of the difference in the magnitude of  $V_o$  and  $V_t$  shall be less than 0.4 volts.  
 The magnitude of the difference in the magnitude of  $V_o$  for one binary state shall be greater than 3.0 volts.

**Fig. 2**  
 Generator Parameter Measurement



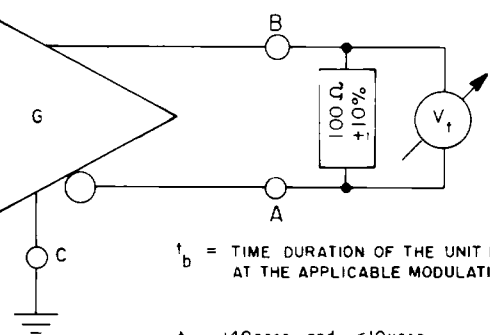
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short circuit measurement shall be made with the generator output terminals shorted to generator circuit ground as illustrated in Fig. 2. The magnitudes of the currents flowing from each generator output terminal during each short-circuit shall not exceed 150 milliamperes for either state.

Power-off measurement shall be made under power-off conditions and as illustrated in Fig. 3. The magnitude of the generator output

leakage currents ( $I_{xa}$  and  $I_{xb}$ ), with voltages ranging between +6.0 and -0.25 volts applied between each output terminal and generator circuit ground, shall not exceed 100 microamperes.

**2.2.5** The output signal waveform measurement shall be made using a test load consisting of a noninductive resistor with a value of 100 ohms  $\pm 10\%$  connected between the generator output terminals, as illustrated in Fig. 3. During transitions of the generator output between alternating

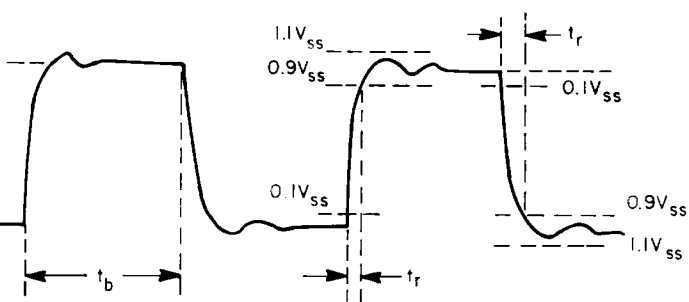


$t_b$  = TIME DURATION OF THE UNIT INTERVAL AT THE APPLICABLE MODULATION RATE

$t_r \geq 140\text{nsec}$  and  $< 10\text{usec}$

$V_{ss}$  = DIFFERENCE IN STEADY STATE VOLTAGES

$$V_{ss} = |V_t - V_t|$$



**Fig. 3**  
Generator Output Signal Waveform

binary states (one-zero-one-zero, etc.), the differential signal measured across the test load shall be such that the voltage monotonically changes between 10% and 90% of  $V_{ss}$  at not less than 140 nanoseconds. Thereafter, the signal voltage shall not vary more than 10% of  $V_{ss}$  from the steady state value, until the next binary transition occurs. At no time shall the instantaneous magnitude of  $V_t$  or  $\sqrt{V_t}$  exceed 6.0 volts nor be less than 2.0 volts.  $V_{ss}$  is defined as the voltage difference between the steady state values of the generator output.

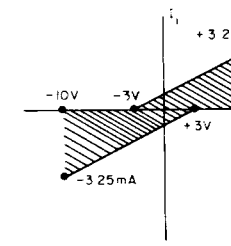
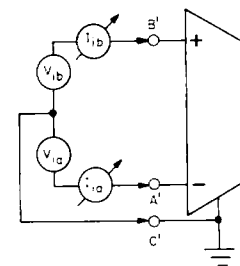
**2.2.6** The generator output shall be capable of being placed in a high-impedance state and when in such state shall withstand a common mode voltage swing of up to 7 volts.

**2.3 Load Characteristics.** The load consists of one or more receivers (R) and an optional cable termination resistance ( $R_t$ ) as shown in Fig. 1. The electrical characteristics of a single receiver excluding both cable termination and fail-safe provision are specified in terms of the measurements described in 2.3.1 through 2.3.7 and illustrated in Figs. 4 through 6. A circuit meeting these requirements results in a differential receiver having a high-input impedance ( $> 4$  kohms), a small input threshold transition region between -0.5 and +0.5 volts and allowance for an internal bias voltage not to exceed 3 volts in magnitude.

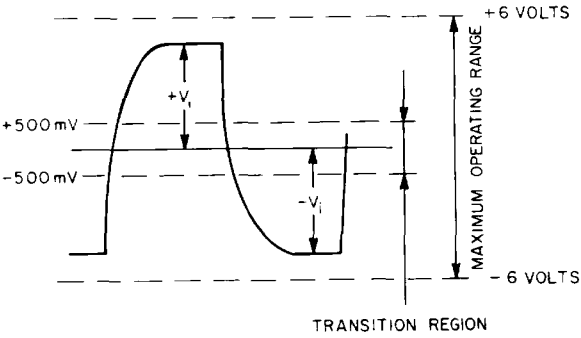
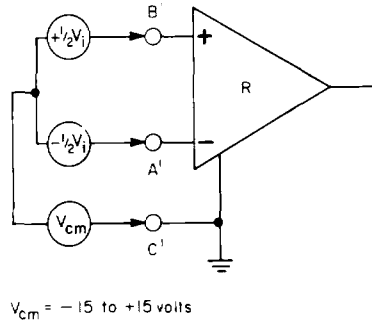
**2.3.1** The input current/voltage measurements shall be made with the voltage via (or  $V_{ib}$ ) ranging between -10.0 and +10.0 volts, while  $V_{ib}$  (or  $V_{ia}$ ) is held at 0.0 volts (ground). This measurement shall be made with the power supply to the receiver in both the power-on and power-off condition. The resultant input current  $I_{ia}$  (or  $I_{ib}$ ) shall remain within the shaded region shown in Fig. 4.

**2.3.2** The input sensitivity measurement shall be made as illustrated in Fig. 5 over the entire common mode voltage ( $V_{cm}$ ) range of -15 to +15 volts. The receiver shall not require a differential input voltage of more than 500 millivolts to correctly assume the intended binary state. Reversing the polarity of  $V_i$  shall cause the receiver to assume the opposite binary state. The receiver is required to maintain correct operation for differ-

ential input signal voltages ranging from millivolts and 6 volts in magnitude. The voltage (signal plus common mode) between either receiver input terminal and circuit ground shall not exceed 7 volts. Application of voltages in excess of the common mode voltage (signal plus common mode) shall not exceed 6 volts or a maximum differential input voltage at the receiver input terminals shall not exceed 6 volts. Operational failure of the receiver in common mode voltage ( $V_{cm}$ ) is defined as the mean of the two voltages at the receiver input terminals ( $A'$  and  $B'$ ) and the receiver circuit ground ( $C'$ ). The receiving hardware should be designed to signal transitions with noise present without instability or oscillatory operation. Appropriate hysteresis should be implemented to prevent such operation. Adequate hysteresis must be implemented to prevent such operation. Adequate hysteresis must be implemented to prevent such operation.



**Fig. 4**  
Receiver Input Current-Voltage



**Fig. 5**  
Receiver Input Sensitivity Measurement

Input balance measurement shall be as indicated in Fig. 6. The balance of the voltage/current characteristics and shall be such that the receiver will be in the intended binary state when a differential voltage ( $V_i$ ) of 500 millivolts is applied. The polarity of  $V_i$  is reversed, the opposite state shall be maintained under the same

use of a noninductive cable termination ( $R_t$ ) is recommended. A distributed or a combined R/C load may be re-

quired in some cases (see 4.2.1) and the use of an active cable termination resistance is desirable for the purpose of reducing cross coupling when the bus controller is placed in a high-impedance state (see 4.2.2). Care must be taken not to exceed the limits on total load resistance or sensitivity. Refer to 2.3.7 for limits on the total load resistance.

**2.3.5** The use of multiple receivers may be employed. Caution must be exercised to avoid performance degradation due to signal reflective effects from stub lines emanating from the load interface point to the receivers.

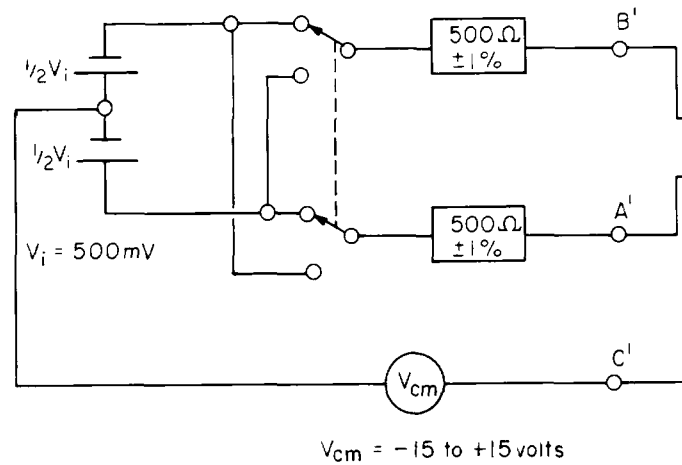
**2.3.6** The interface system shall fail safe. This shall be accomplished by automatic disconnection of a tributary from the interface system in the event of a malfunction or power failure and incorporating in the receiver provisions to provide a steady binary MARK to protect against the following conditions:

Generator power-off

Generator in high-impedance state (Both signal wires open or shorted to common return still connected)

Generator not implemented (Signal wires may not be present)

Open connector (Both signal wires open or shorted to common return are open or shorted)



**Fig. 6**  
Receiver Input Balance Measurement

**2.3.7** The total load characteristics, including multiple receivers, fail-safe provision, and cable termination shall have a combined resistance greater than 90 ohms between its input points (A' and B' [Fig. 1]) and shall not require a differential input voltage of more than 500 millivolts for all receivers to assume the intended binary state.

**2.4 Interconnecting Cable Characteristics.** The physical and electrical characteristics of the interconnecting cable are given in 2.4.1 through 2.4.4 with additional guidance given in Sec. 4. An interconnecting cable conforming to this standard will result in a transmission line with a nominal characteristic impedance in the order of 100 ohms at frequencies greater than 100 kilo-

hertz, and a DC series loop resistance of 240 ohms over an operating length of nominally 1220 m. The cable shall be composed of twisted or nontwisted (flat) conductors possessing the characteristics specified in 2.4.4. Most common cable used for telephone applications shall meet these specifications.

**2.4.1** Each conductor of the interconnecting cable shall be composed of solid copper wire whose uniformity of diameter is 24 AWG or larger. The conductor is allowed of sufficient size to yield a DC resistance not exceeding 30 ohms per 1000 m.

pair capacitance, that is, the capacitance between one wire in the pair and the other wire in the pair, shall not exceed 20 picofarads, and the value shall be reasonably uniform over the entire length of the cable.

capacitance, the capacitance between one wire in the cable and all others in the cable with all others connected to ground, shall not exceed 40 picofarads per ft and shall be reasonably uniform over the entire length of the cable for any given conductor.

Inter-pair balanced crosstalk is defined as the ratio of the voltage induced in one pair of wires in the same cable. This shall be attenuated a minimum of 40 dB at 150 kHz with each cable pair terminated in its characteristic impedance.

Balance. A balance voltage digital interface conforming to this standard will be tested at a data rate of 38.4 kb/s and the following operational constraints shall be simultaneously observed.

Interconnecting cable length is a nominal length of 20 m and the cable is appropriately terminated.

Common mode voltage at the receiver is less than 100 mV (peak). Common mode voltage is the result of any uncompensated combination of generator/receiver ground potential difference, generator offset voltage (Vos), and the induced common mode voltage coupled between the receiver circuit and the generator circuit, with the generator end of the cable terminated to ground.

Protection. The balanced-voltage digital interface generator and receiver device, when in power-on or power-off condition and when tested in accordance with this standard, shall not be damaged under the following conditions:

Open circuit  
Short circuit across the balanced interconnecting cable

Connection to any other lead using electrical connections in compliance with this standard shall be terminated to ground

(The above faults may cause the power dissipation in the interface device to approach the maximum power dissipation tolerable by a typical integrated circuit (IC) package. Caution should, therefore, be exercised when multiple generators or receivers are implemented in a single IC package since only one such fault per package may be tolerated at any one time without experiencing IC failure. It should also be noted that the generator and receiver device(s) complying with this standard may be damaged by spurious voltages applied between the input/output terminals and circuit ground. In applications where the interconnect cable may be subject to severe electromagnetic environment or the possibility exists that it may be inadvertently connected to circuits not in compliance with this standard, additional protection should be employed as may be appropriate.)

### 3. Mechanical Characteristics

**3.1 Interface Connector.** The interface connector shall be a 9-pin D-subminiature female (DB-9S). A single interface connector shall be associated with any particular tributary device. Multiple interface connectors may be utilized on a bus controller in the case of a multipoint system or when the bus controller must communicate with more than one interface system.

**3.2 Pin Assignment.** The pin assignments for the bus controller and tributary shall be as shown in Fig. 7. Use of the spare pin for unspecified communication or supervision is not in compliance with this standard. If used, it may not interfere with the normal operation of the standard interface system.

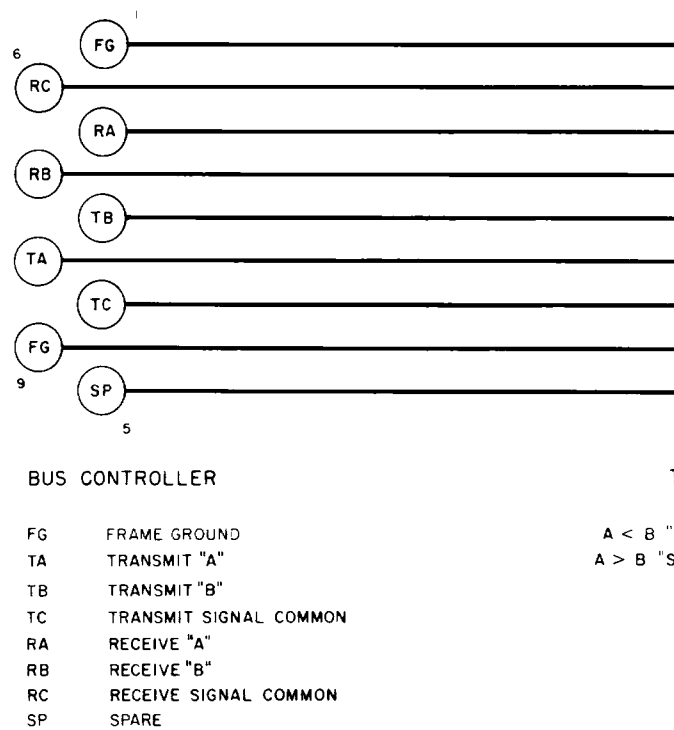
### 4. Guidelines

When interconnecting equipment using the interface system described in this standard, consideration should be given to some of the problems that may be encountered due to the characteristics of the interconnecting cable, cable termination, the number of devices in use, and grounding arrangements.

**4.1 Cable.** The interconnecting cable electrical characteristics are specified in 2.4. The following is intended to be used as additional guidance when considering the operational constraints placed on the system by the cable parameters.

**4.1.1** The maximum length of cable separating the generator and receiver (load) is a function of modulation rate (influenced by the tolerable signal distortion), transmission losses, the amount of longitudinally coupled noise, and ground poten-

tial difference introduced between generator and receiver circuit grounds and ground balance. Increasing the physical length of interconnecting cable length increases the system exposure to noise, signal distortion, and ground imbalance. Users are advised to minimize length to the minimum consistent with the generator/receiver (load) separation whenever possible to utilize cable designed for balanced data circuits.



**Fig. 7**  
Connector Pin Assignment

4.2.2 The presence of stray capacitance between the interconnect cable and any adjacent cable (Fig. 8) can result in interference being coupled to an adjacent cable when a transition occurs that is other than balanced. During normal operation, inter-cable coupling is at a minimum due to the use of a balanced transmission mode along with control of signal rise-times (2.2). When the driving device is placed in a high-impedance state, however, this control is no longer applied and the conductor in the pair that was at a positive value will transition to a less positive value. This transition, being uncontrolled and of an unbalanced type, may be coupled into adjacent cables.

Capacitive coupling of this type can be reduced or eliminated by utilizing shielded cables specifically designed for the transmission of digital data information. Although this approach is practical when installing the interface system in new plants, it may not be possible when working in existing facilities. When utilizing nonshielded cable, the use of an active termination is recommended. An active termination of the type shown in Figs. 9 and 10 will result in a balanced transition to a voltage that is equal on both conductors of the cable pair. The circuit shown in Fig. 9 also provides a fail-safe bias on the bus and allows for higher impedance terminations with respect to the interface bus and does not introduce a differential bias on the line.

4.2.3 In general, reliable operation of the balanced interface circuit is not particularly sensitive to the presence or absence of the cable termination resistor when operating at 38.4 kb/s. Load in the order of 90 to 250 ohms tends to result in the preservation of the rise time in the generated signal and a reduction of line noise. Current must be exercised in the value of termination selected as too low a value would result in a reduction in signal amplitude to the point where reliable operation of the system would be affected.

4.2.4 The data rate of 38.4 kb/s can result in a system response time within one television frame when the total number of tributaries is less than thirty-two. Higher data rates may be used when the operation of a specific system indicates this need. When higher data rates are used, the device(s) shall first establish communication at a rate of 30 kb/s. Operation at data rates less than 30 kb/s is expressly prohibited and confusion of certain data BREAK sequence.

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Fig. 9 Terminator Circuit 1

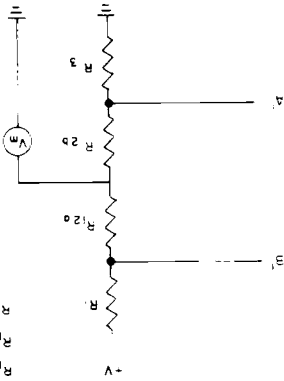
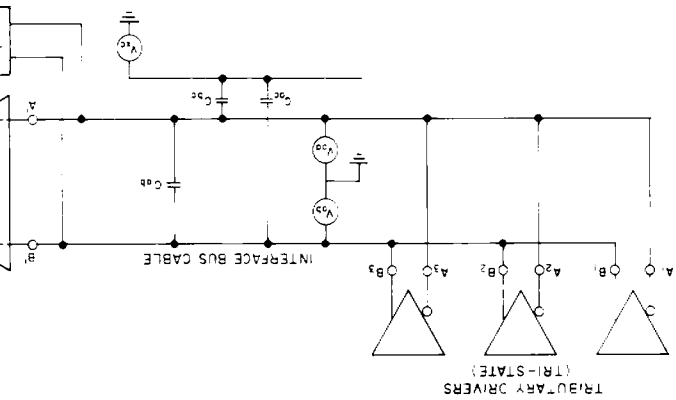


Fig. 8 Cable Model



$R_{12} + R_{12b}$  ARE USUALLY COMBINED  
 $R_{12} = R_{12a} + R_{12b}$  ALSO  $R_{12a} + R_{12b}$   
 $R_{11} \gg R_{12}$   $R_{13} \gg R_{12}$

Fig. 7 Terminator

