

Technology Report— A Proposed 10 Gbit/sec Interface

The following report represents a contribution from Sony Corporation to the SMPTE N26 Study Group investigating High-bandwidth Interfaces under the chairmanship of Johann Safar. It is likely that the principles outlined in this report authored by Kazuhiro Takano and Shigeyuki Yamashita of Sony Corp. will become the basis for a future SMPTE standard. The Study Group recognizes that this approach may not be the only approach, and that other proposals are encouraged. The need for higher bandwidth interfaces is required to address the imminent needs of the D-Cinema community, and the introduction of 1920 x 1080 x 60p image formats into the marketplace.

Introduction

It is now almost 20 years since the first SDTV serial interface was standardized as SMPTE 259M. This serial interface enabled the initial success of digital television. The 1.485 Gbit/sec serial digital interface for 1920 (H) x 1080 (V) images was standardized as SMPTE 292M in 1996 and is now widely known as HD-SDI. Today these two interfaces provide the basis for all digital systems design.

With advances in technology and the imminent commercial availability of 1920 x 1080 x 60P progressive equipment along with D-Cinema application, the requirement exists for a higher bit rate interface. One approach is to operate the current interface with what is called dual link connections (standardized as SMPTE 372M). Another is to multiplex the dual link data mappings into a single 3 Gbit/sec dual link.

The 3 Gbit/sec approach, while very practical, does not cover all the potential applications that are now emerging. The D-Cinema application, while constrained to 24 or 48 frames/sec, uses a sampling strategy of 4:4:4 with a pixel depth of 12 bits, and may be more in the acquisition stages. Likewise, the TV production industry is now using 50/60 Hz frame rates at pixel depths of 12 bits. In some of these applications, the uncompressed bit rates exceed the 3 Gbit/sec limit imposed by the dual link approach.

The SMPTE Study group on High Rate Interfaces has been looking into potential technologies that would meet the requirements of the D-Cinema and TV industry for the foreseeable future. One proposal, as described in this report, supports a 10 Gbit/sec interface while still maintaining many of the characteristics of the current serial interfaces and also providing for bidirectional connections.

There is no best solution; there are always tradeoffs, and “best solutions” can be expensive. For this proposal only commercially available parts have been proposed to keep costs as low as possible while providing flexibility.

User Requirements

The minimum user requirements for the next-generation realtime interface are summarized as follows:

1. Its payload bandwidth should be a minimum of 4096 (H) x 2160 (V) x 12 bit x 3 ch (XYZ) x 24 (Hz) = 7.64 Gbits/sec in order to transmit a 4k x 2k signal plus synchronization and audio signals.
2. A robust channel coding having a transition-rich and DC-balanced code for the transmission media should be adopted.
3. A transmission distance up to 2 to 3km is required to broadcast baseball games or golf tournaments.
4. Currently used 1.3 μ m single-mode fiber cables and the Camera Optical Fiber should be used.
5. Use of existing high-speed interface technology where applicable for the widespread adoption of the interface. Of particular interest has been the development of the 10 Gigabit Ethernet interface (10GE).
6. Consideration should be given to TV applications as well as D-Cinema applications.

Basic Concepts

The proposed 10 Gbit/sec realtime interface is a low delay realtime interface that has the same data structure as SMPTE 292M, although it uses the robust channel coding 8B/10B instead of the scrambling employed for the HD-SDI implementation. It covers the 4k x 2k/24P signal and all the signal formats defined in SMPTE 274M and SMPTE 296M. It is designed to have the flex-

Transmission module for 10Gbps

■ XFP MSA v3.1

XFP is used for

- OC192/STM-64 9.95 Gb/s
- ITU-T G.709 10.7 Gb/s
- IEEE802.3ae 10.3 Gb/s (10 Gigabit Ethernet)
- 10 Gigabit FC 10.5 Gb/s

And...

- 10Gb/s-SDI 10.69Gb/s



Description	Specification
Dimension	78 × 18 × 8 mm
Power Consumption	2 W (Transceiver)
LASER wavelength	1,310 nm

Figure 1. XFP optical transceiver.

ability to be a transmitter, a receiver, or a transceiver depending on the application.

Available 10 Gbit/sec devices such as the XFP are used in order to achieve the low power and low price interface. The XFP is the smallest size and lowest power optical transceiver developed for the 10GE, 10G Fibre channel and the SONET/SDH. By adopting a 1.3µm wavelength XFP, a transmission distance up to 2 to 3km is achieved; the same as the 1.5 Gbit/sec HD-SDI optical interface (Fig. 1).

Technologies used in the “10 Gbit/sec Realtime Interface”

Realtime Synchronous Interface

The realtime and synchronous 10 Gbit/sec interface was realized by selecting a clock frequency of 10.692 Gbits/sec that is 144 times the 74.25 MHz parallel clock frequency of the HD-SDI.

At the 10G transmitter side (10G_TX), signal processing is performed by a 74.25 MHz clock recovered from the HD-SDI source and the synchronous 10.692 Gbit/sec serial signal is created and transmitted. The parallel clock frequency of 74.25 MHz (or 74.25/1.001 MHz) is detected automatically.

At the 10G receiver side (10G_RX), signal processing is performed by the clock recovery circuit to obtain a synchronized 10.692 GHz clock from the 10.692 Gbit/sec input signal, and HD-SDI clocks at 74.25 MHz are created by division of the 10.692 GHz clock.

Since most of the 10 Gbit/sec devices run at between SONET/SDH 9.9532 Gbits/sec and SONET/SDH+FEC 10.709 Gbits/sec it is expected that the ICs and XFP module used will be at a lower price in 2 to 3 years.

Block diagram for the 10Gbps interface

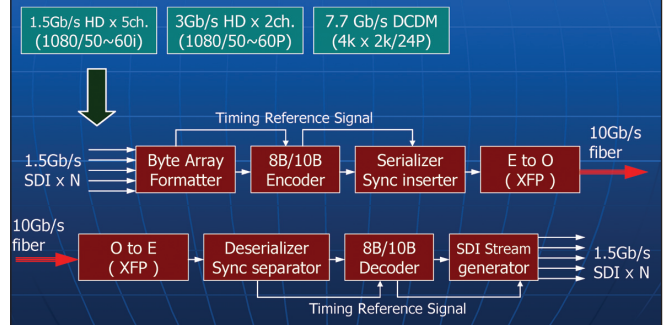


Figure 2. Block diagram of the signal processing.

Signal Processing at 10G_TX

Figure 2 shows the block diagram of the signal processing of the 10G realtime interface. The I/O for the 10G realtime interface are multiple channels of 1.5 Gbit/sec SDI that comply with SMPTE 292M or SMPTE 372M. When the 1080/50P-60P, the 2k x 1k/24P, 48P or the 4k x 2k/24P signals are to be transmitted, they need first be mapped into multichannel HD-SDI format. If audio signals or other ancillary signals are to be added, these signals should be mapped into the H-Blank or V-Blank area of the HD-SDI interfaces as ancillary signals conforming to SMPTE 291M. The 10G realtime interface does not provide for the mapping function of ancillary signals in order to reduce size, but it can transmit the ancillary signals that are present in the H-Blank or V-Blank area of HD-SDI with some restrictions. The 2k x 1k/24P images being standardized in SMPTE DC28 needs to be mapped into the revised version SMPTE 372M (currently in ballot within the SMPTE N26 Technology Committee). Up to four channels of 2k x 1k images can be packed for transmission by this method. The 4k x 2k/24P signal needs to be mapped into the four channels of the revised version SMPTE 372M for input to the 10G realtime interface. In this way, compatibility with the revised version SMPTE 372M can be achieved.

The robust channel coding of 8B/10B was adopted to have a transition-rich and DC-balanced code. First, multichannel HD-SDI inputs are S/P (serial to parallel) converted using the SAV codes present in each line, and the CRCC error of each channel is detected. After S/P conversion, the number of samples of one horizontal line (H_CNT) is counted so that the frame rate and the HD formats of 1080P or 720P can be recognized. The

Applications beyond 1.5Gb/s

■ Applicable image formats

Input Video	Sampling Structure	Quantization	Frame Rate	Payload Bit Rate
4k x 2k DCDM			24P	10.7Gbps
2k x 1k DCDM	4:4:4 XYZ	12 bit	48P	1.5Gbps x 4
2k x 1k DCDM			24P	1.5Gbps x 2
1080/50P,60P	4:4:4 RGB	10 or 12 bit	50P, 60P	1.5Gbps x 4
1080/50P,60P	4:2:2 YC _B Cr	10 bit	50P, 60P	1.5Gbps x 2
1080/60i etc. (Full Bit 5ch.)	4:2:2 YC _B Cr	10 bit	24P,25P, 30P 50i,60i	1.5Gbps x 5

Note: 720/50P~60P can be also embedded in 5 channel mode.

Figure 3. Applicable image formats.

signal processing is automatically switched depending on this H_CNT value. A state machine is constructed for the forward and backward protection by detecting the SAV codes and the H_CNT.

Once the sync-established state has been reached, 8B/10B encoding process starts. First, multichannel HD-SDI inputs are S/P (serial to parallel) converted using the SAV codes present in each line, the data is then subject to 8B/10B encoding and input to RAM memories. When a single image format, such as 1080/50P,60P or 4k x 2k/24P is the input signal, the phase of each HD-SDI is aligned using the RAM buffers. Since these RAM buffer have a memory size of one horizontal line data, phase adjustment up to ± 1/2 horizontal line is possible. At the sync inserter, 2 bytes of K28.5 special character and 1 byte of data flag are inserted in place of the SAV code of the HD-SDI first channel for the byte boundary detection of 8B/10B code and for recognition of the number of the active samples, either 2048 or 1920 (4096 or 3840) at the 10G receiver. Signal processing on a per-line basis has minimized memory requirement and the delay due to the 10G_TX plus 10G_RX signal processing is about one horizontal line period mainly due to the phase alignment at the 10G_TX RAM buffer.

In each transmission mode, the V-Blank area is not deleted in order to reduce the RAM memory size and the delay due to the signal processing. Finally, these phase aligned signals are multiplexed up to 10.692 Gbits/sec and is input to the XFP. The XFP then converts the incoming serial electrical signal to the optical signal.

Signal Processing at 10G_RX

At the 10G receiver, signal processing is a mirror of the 10G transmitter side processing. First, the XFP con-

Line structure of 1.5Gb/s SDI@30Hz

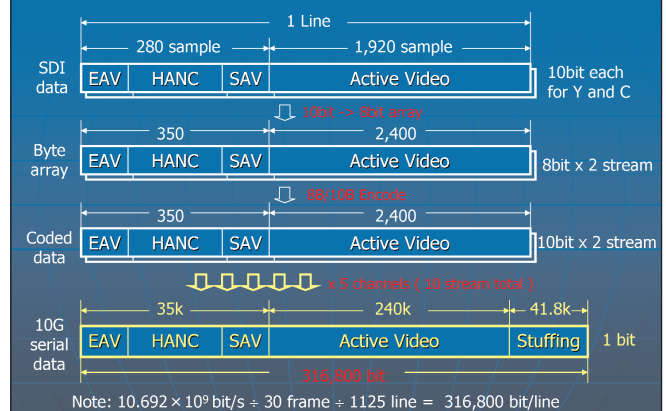


Figure 4. Line structure of 1.5 Gbits/sec HD-SDI 5-channel.

verts the 10.692 Gbit/sec optical signal to an electrical signal and this serves as input to the deserializer. At the deserializer, 2 bytes of K28.5 are detected to search the byte boundary of the 8B/10B codes. A state machine that is the same as the 10G_TX state machine is constructed for the forward and backward protection by detecting the two bytes of K28.5 and the number of samples of one horizontal line of the 10G data.

After establishing clock and deserializer synchronization, incoming data is 8B/10B decoded and the data flag detected. The data flag is used to indicate the input video formats on the 10G realtime interface and the active sample numbers of 2048 or 1920 (4096 or 3840) in case the signal formats are the 2k x 1k/24P, 48P or the 4k x 2k/24P. The 10G realtime interface can cover not only the active areas of 2048 and 4096 pixels but also 1920 and 3840. The SAV codes of the HD-SDI first channel are restored to the original 3FFh, 3FFh, 000h, 000h, 000h, 000h and any CRCC error is detected. Finally, the HD-SDI data streams are created using the 8B/10B decoded data and the 74.25 MHz clock (divided from the 10.692 GHz recovered clock).

CPU, I2C and JTAG Interface

The FPGA is equipped with a CPU interface, a I2C interface and a JTAG interface so that it can communicate with the XFP synthesizers and the system CPU through these interfaces. It is possible to rewrite the FPGA program of the system CPU with the JTAG interface. The status of the XFP such as the laser output power, the received optical power, temperature, lock conditions of synthesizers, the frame rates and the CRCC error of the HD-SDI at the 10G_TX and 10G_RX etc., are registered by the FPGA and reported to the system CPU through these interfaces.

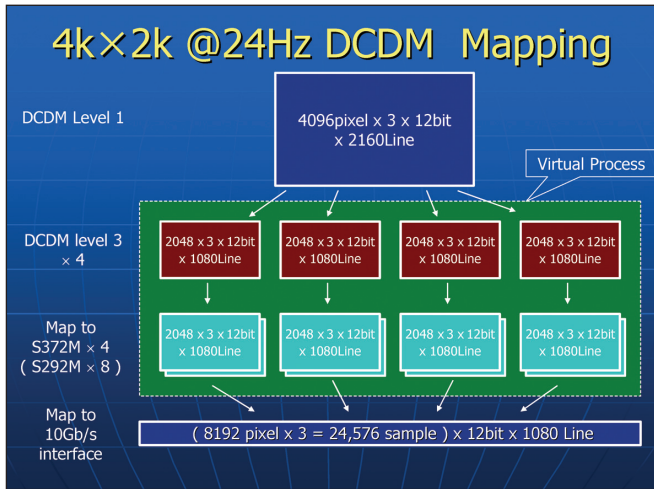


Figure 5. 4k x 2k/24P mapping to multichannel HD-SDIs.

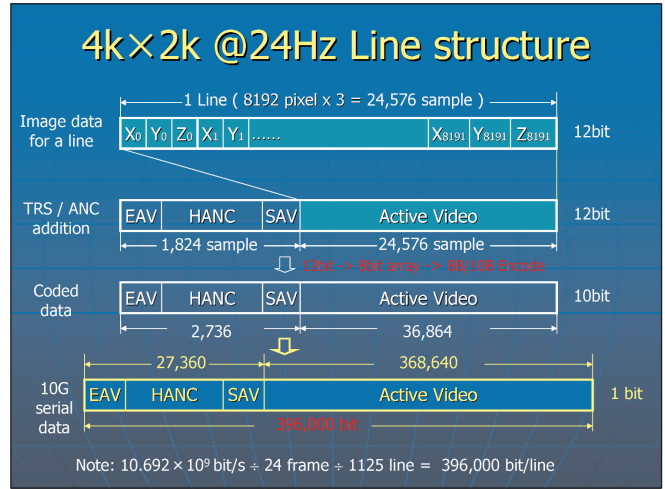


Figure 6. Line structure of the 4k x 2k/24P signal.

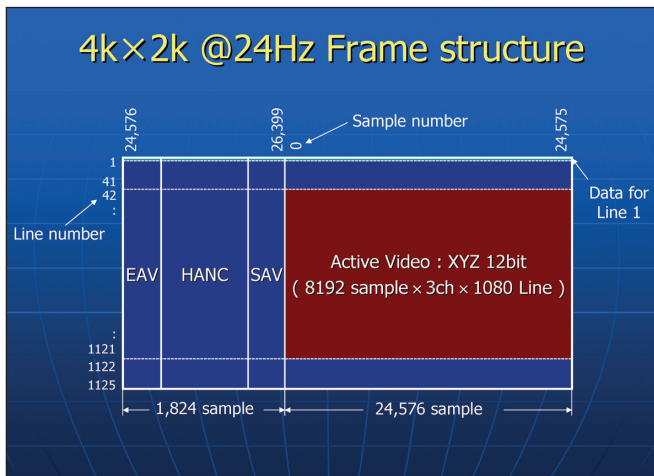
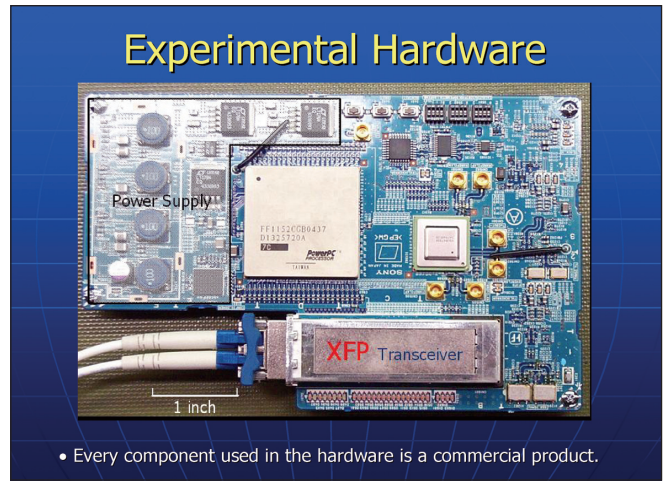


Figure 7. Frame structure of the 4k x 2k/24P signal.



• Every component used in the hardware is a commercial product.

Figure 8. Hardware board.

Synthesizers

The 10G realtime interface is equipped with three types of synthesizer so that it has flexibility to lock to the incoming HD-SDI when it runs as a transmitter or transceiver, or to the incoming 10.692 Gbit/sec signal when it runs as a receiver or transceiver. For example, the 10G realtime interface for the 4k x 2k/24P transmitter runs by locking to the first incoming HD-SDI channel of the eight channels of HD-SDI to which 4k x 2k/24P signal is mapped. Conversely, the 4k x 2k/24P receiver runs by locking to the incoming 10.692 Gbit/sec serial signal.

Applicable Image Formats

As shown in Fig. 3, the interface can transmit the 4k x 2k/24P signal and all the signal formats defined in SMPTE 274M and SMPTE 296M. It can also transmit up to five channels of HD-SDI uncompressed. If all five channels are synchronized to the 74.25 MHz master

clock, the frame rate of each channel may be different. For example, if the first channel was 30P, any frame rate of 24P, 25P, 50I, 30P or 60I of the second, the third, the fourth, and the fifth channel can be mapped independently. In addition to this, even if a HD-SDI signal is not input to the second, third, fourth, and fifth channel, it can still operate as long as there is a HD-SDI input for the first channel.

Figure 4 shows the line structure of the 10G realtime interface for the HD-SDI five-channel mode. Figure 5 shows how to map the 4k x 2k/24P signal onto the multichannel HD-SDI. Figures 6 and 7 show the line and the frame structure for 4k x 2k/24P signals. Since the I/O stream for the 4k x 2k/24P signal is HD-SDI at 24 frames/sec, the frame rate of the 10G realtime interface is also 24 frames/sec and has SAV/EAV codes as synchronization signals defining 1125 active lines per frame. Ancillary signals such as the audio signal can be

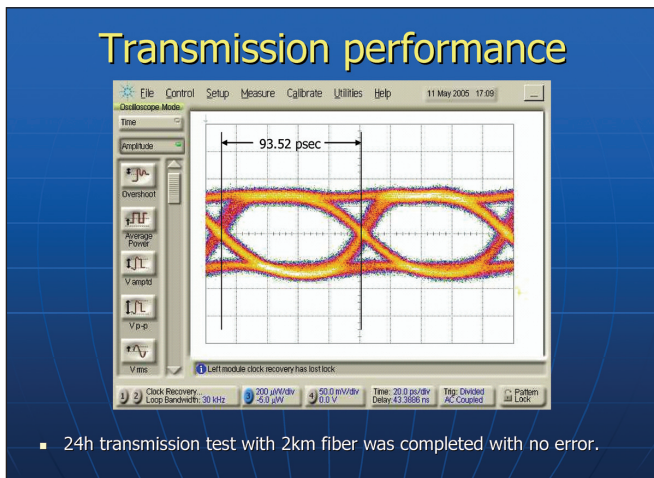


Figure 9. Optical eye diagram from XFP.

embedded into the H-Blank or V-Blank area of the virtual HD-SDI first channel and these ancillary data are mapped into the H-Blank or V-Blank area of the 4k x 2k/24P frame structure as shown in Fig. 7.

Signal Integrity

The 10G realtime interface board is shown in Fig. 8. The 10 Gbit/sec serial signal propagates through the conventional Halogen-Free multilayered FR-4. The board thickness is 2mm and has 12 layers. All the ICs, such as FPGA, synthesizers, DC-DC converters etc., and the XFP module are integrated into this board giving an overall size of about 100mm x 150mm. Figure 9 shows the 10 Gbit/sec optical eye diagram from the XFP and shows the clear eye opening.

Conclusion

A “10G Realtime Interface” is being proposed to

SMPTE Technology Committee N26. It addresses the following issues:

1. A data structure and signal processing that can cover 4k x 2k/24P signal as well as all the signal formats defined in SMPTE 274M and SMPTE 296M.

2. A frequency synthesizer that has flexibility to be locked to the incoming HD-SDI (Transmitter/Transceiver mode), or to the incoming 10.692 Gbit/sec signal (Receiver/Transceiver Mode).

3. The signal integrity required to transmit 10 Gbit/sec serial electrical signal through a conventional multilayered FR-4.

4. A reasonable price using conventional 10 Gbit/sec devices.

In order to achieve a low-power unit, a low-cost 10G realtime interface and to promote the spread of this interface, the 10G realtime interface being proposed makes good use of readily available 10 Gbit/sec devices. These devices, although currently expensive, should decrease in cost following the spread of SONET/SDH and 10GE into their markets so we believe 10G realtime interfaces can be manufactured at a comparatively low cost. The stability of the transmission signal was secured by adopting 8B/10B channel coding. A transmission distance up to 2 to 3km has been achieved using conventional camera optical fiber by adopting a 1.3 μ m wavelength XFP to achieve the same transmission length as the HD-SDI optical interface. This 10G interface is proposed as the next-generation realtime interface that can cover all the signal formats in SMPTE 274M and SMPTE 296M as well as the 2k x 1k/24P, 48P or 4k x 2k/24P signals being standardized in SMPTE DC28. It also maintains backward compatibility with SMPTE 292M and SMPTE 372M.

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Shigeyuki Yamashita joined Sony Corp. in 1984, where he has been engaged in the development of high-speed electrical and optical serial interface for high-definition video equipment. He promoted the standardization of SMPTE 292M in 1996 and SMPTE 372M in 2002. He is

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